INCH-POUND
MIL-PRF-22885/117B
5 August 2024
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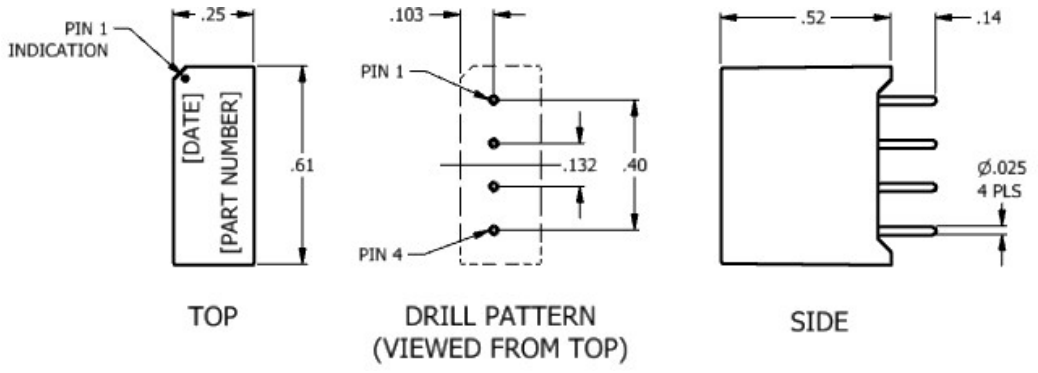
24 November 2023

PERFORMANCE SPECIFICATION SHEET

SWITCH, PUSHBUTTON, ACCESSORY, OPTIONAL ELECTRONIC COMPONENT (OEC), SWITCHING AND LOGIC FUNCTION, LOW LEVEL, STAND-ALONE THROUGH HOLE-SOLDERABLE, AND COMMON TERMINATION SYSTEM (CTS) COMPATIBLE WITH MIL-PRF-22885/108 AND MIL-PRF-22885/113 PUSHBUTTON SWITCHES AND MIL-PRF-22885/116 MODULE

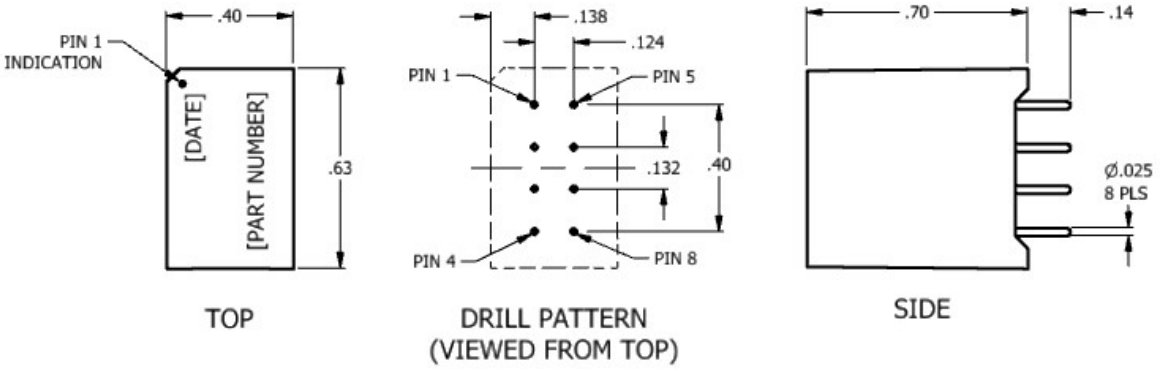
This specification is approved for use by all Departments and Agencies of the Department of Defense.

The complete requirements for acquiring the switches described herein shall consist of this specification and the latest issue of MIL-PRF-22885.



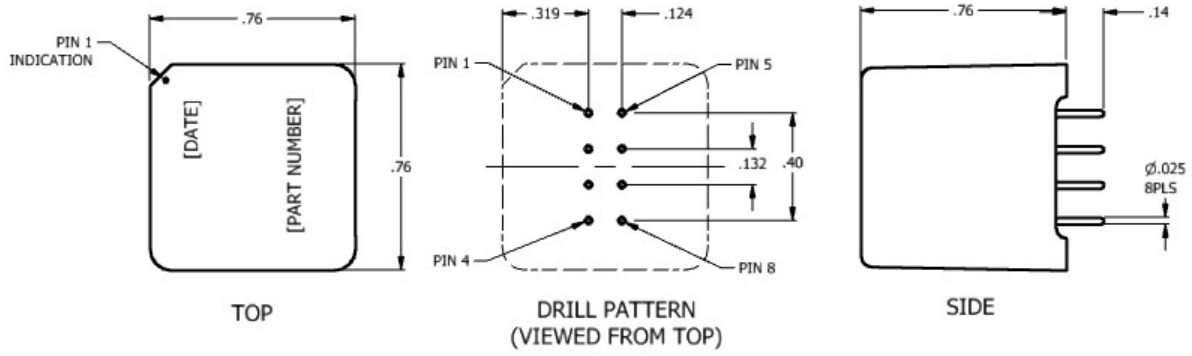
NOTES:
1) Unless otherwise noted, all dimensions are in inches. The tolerance is +/- 0.005 for three decimals and +/- 0.010 for two decimals.
2) Component Dimensions shown in this figure are for solderable OECs only.
3) For OECs installed in enclosures defined by MIL-PRF-22885/108, /113 and /116, dimensions, pin size, pin nomenclature, pin spacing, and component size is determined by enclosure type and the compatibility to the corresponding Common Termination System (CTS).

FIGURE 1. Series A OEC, Solderable.



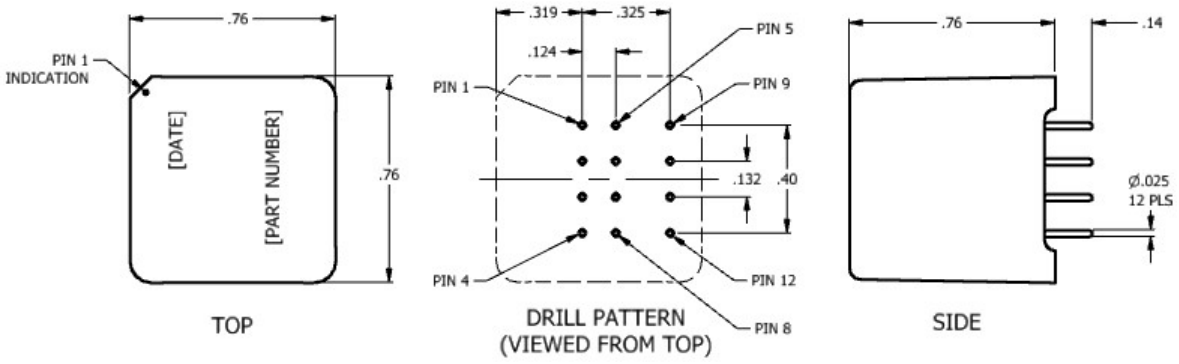
NOTES:
1) Unless otherwise noted, all dimensions are in inches. The tolerance is +/- 0.005 for three decimals and +/- 0.010 for two decimals.
2) Component Dimensions shown in this figure are for solderable OECs only.
3) For OECs installed in enclosures defined by MIL-PRF-22885/108, /113 and /116, dimensions, pin size, pin nomenclature, pin spacing, and component size is determined by enclosure type and the compatibility to the corresponding Common Termination System (CTS).

FIGURE 2. Series C OEC, Solderable.



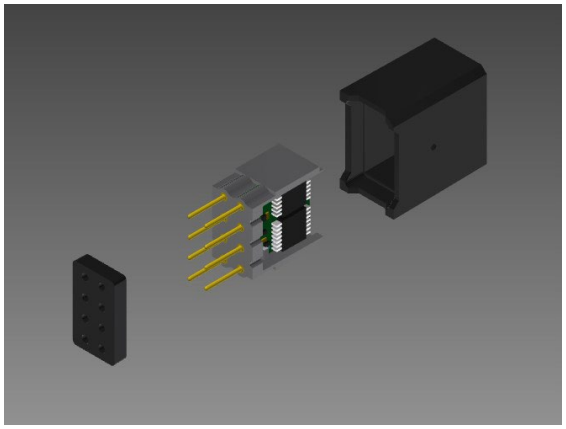
NOTES:
1) Unless otherwise noted, all dimensions are in inches. The tolerance is +/- 0.005 for three decimals and +/- 0.010 for two decimals.
2) Component Dimensions shown in this figure are for solderable OECs only.
3) For OECs installed in enclosures defined by MIL-PRF-22885/108, /113 and /116, dimensions, pin size, pin nomenclature, pin spacing, and component size is determined by enclosure type and the compatibility to the corresponding Common Termination System (CTS).

FIGURE 3. Series N OEC, Solderable.



NOTES:
1) Unless otherwise noted, all dimensions are in inches. The tolerance is +/- 0.005 for three decimals and +/- 0.010 for two decimals.
2) Component Dimensions shown in this figure are for solderable OECs only.
3) For OECs installed in enclosures defined by MIL-PRF-22885/108, /113 and /116, dimensions, pin size, pin nomenclature, pin spacing, and component size is determined by enclosure type and the compatibility to the corresponding Common Termination System (CTS).

FIGURE 4. Series R OEC, Solderable.



NOTES:
1) Housing and Cover are not required for OECs installed in enclosures defined by MIL-PRF-22885/108, /113 and /116.
2) Electronic PCB assembly, functional and electrical characteristic of Solderable OEC and OEC inside MIL-PRF-22885/108, /113 and /116 are the same.

FIGURE 5. Generic Exploded view of the assembly.

TABLE I. Optional Electronic Components (OECs).

Operating info in Tables	Optional Electronic Component (OEC) Function	Series	Mfg. ID	Mil ID	Extended ID
II thru IV	Solid State Relay	A	SSR	SR	1H
					1M
					1L
					2H
					2M
					2L
					3 3/
V thru VIII	Combination- Solid State Relay 1/	C	SSRC	CR	
IX thru XI	Voltage Sensor 1/	A	VS	VS	A
					B
XII thru XIV	Diode Pack	A	DP	DP	C
					M
XV, XVI	Terminal Block	A	TB	TB	
XVII thru XXI	Electronic Latch	C	EL	EL	1
					2
XXII thru XXVI	Electronic Rotary	C	ER1	ER	1
XXVII thru XXXI	Pulse Timer 1/	C	PT1	PT	1
XXXII thru XXXIV	Current Sensor 1/	A	CS	CS	
XXXV thru XXXVIII	Time Delay 1/	A	TD	TD	1
					2
XXXIX thru XLII	Square Wave Oscillator 1/	A	CT	CT	1
					2
XLIII thru L	Defined Logic 1/	C	DL	DL	1
					2
					3
					4
LI thru LXX	ARINC Single-Bit Converter 1/	N	SR429/1M	SC	
	ARINC Multi-Bit Converter 1/ 2/	N or R	SR429/4M	MC	
	ARINC Multi-Bit Binary Decoder 1/ 2/	N or R	SR429/4D	MD	
	RS232/RS422 Converter	N	RS422	RS	

1/ These OEC have configurable options after the Extended ID that will only be reflected on manufacturer part numbers.
2/ These OEC can be series N or R depending on the outputs.
3/ The product is only available in the MIL-PRF22885/108, MIL-PRF22885/113, and the MIL-PRF22885/116 form factor.

Solid State Relay (single), Specifications:

Solid State Relays (SSR) are Series-A (4 Pin) components. SSR allows custom digital and analog signal control, as well as audio and data transitions.
The SSR electrical circuit includes Signal Buffering, Optical Isolation, and Surge-Suppression, between inputs and outputs, to provide control circuit isolation and to protect it from load transients. The SSR control circuit is bridge rectified and therefore bi-directional, allowing DC voltages to be applied in either polarity. See Figure 6.

TABLE II. Configuration (SSR).

	28 VDC	14 VDC	5 VDC
Normally Open (NO): 0.75 Amp (Resistive) max output load capacity 1/	SSR1H	SSR1M	SSR1L
Normally Closed (NC): 0.25 Amp (Resistive) max output load capacity 1/	SSR2H	SSR2M	SSR2L
Normally Open (NO) 5 Amp (Resistive, Inductive Motor) max output load capacity	SSR3	-	-

1/ The outputs switch up to 32 VDC or 28 VAC RMS and are surge-protected against transients and overload conditions via a MOV and fast-blow fuse. 1.6 A for Normally Open and 0.5 A for normally Close.

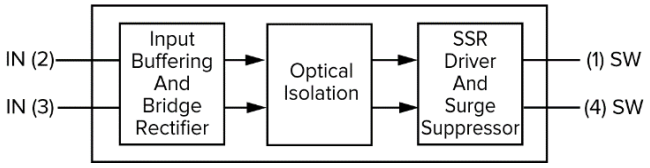


FIGURE 6. SSR.

TABLE III. Input Parameters (SSR).

	SSR1H/SSR2H	SSR1M/SSR2M	SSR1L/SSR2L	SSR3
Max. Voltage ON	32 VDC	18 VDC	6 VDC	32 VDC
Nominal Voltage ON	28 VDC	14 VDC	5 VDC	28 VDC
Min. Voltage ON	18 VDC	8 VDC	4 VDC	18 VDC
Voltage Off (max)	+6 VDC	+4 VDC	+2 VDC	+6 VDC
Typical Operating Current	6.3 mA	6.2 mA	12.1 mA	10 mA
Typical Input Impedance	4.4Kohms	2.2Kohms	400 ohms	2.8 Kohms
Turn On Time Max	5 ms / 1 ms	5 ms / 1 ms	5 ms / 1 ms	5 ms/ 1 ms
Turn Off Time Max	0.5 ms / 3 ms	0.5 ms / 3 ms	0.5 ms / 3 ms	0.5 ms/ 3 ms

TABLE IV. Output Parameters and Load Capacity (SSR) 1/.

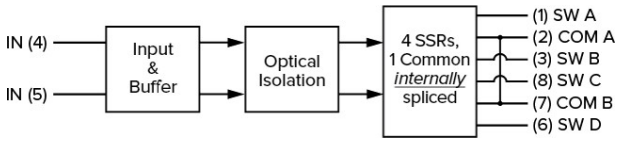
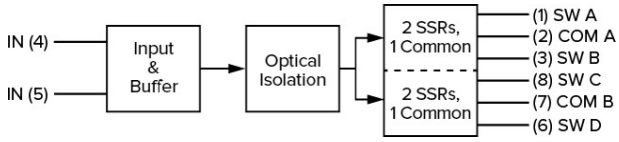
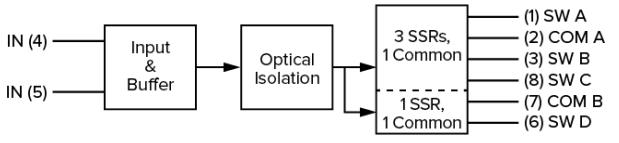
	SSR1 (NO)	SSR2 (NC)	SSR3 (NO)
Max. Output Voltage	32 VDC or 28 VAC		32 VDC
Min. Output Voltage	N/A		18 VDC
Loads (AC/DC):			
On Resistance	Typical 0.2-ohm Max 0.5 ohm	Typical 1.0-ohm Max 2.5 ohm	25 mOhms
Resistive	0.75 A	0.25 A	5 A (DC only)
Inductive	0.5 A (300mH)	0.25 A (300mH)	5 A (DC only)
Lamp	0.1 A(1A, 10ms. Inrush)	N/A	N/A
Audio	< 600 ohms		N/A
Motor	N/A	N/A	5 A (DC only)
Temperature Operating	-55 C to 85 C		
Temperature Non-Operating	-55 C to 85 C		

1/ Load tests performed at +85° C.

Combination- Solid State Relay (SSR-C), Specifications:

Combination-Solid State Relays (SSR-C) are Series-C (8 Pin) components. SSR-C shall allow three switching configurations with multiple combinations of Normally Open (NO) and Normally Closed (NC) relays.

TABLE V. Configurations (SSR-C).

	28 VDC	Commons
SSRCH/ABCD 1/ 2/		4 SSRs with a single common spliced internally
SSRCH/AB/CD 1/ 2/		2 SSRs connected to common A and 2 SSRs connected to common B
SSRCH/ABC/D 1/ 2/		3 SSRs connected to common A and 1 SSRs connected to common B

1/ Each character of ABCD is replaced with either 1 for NO (Normally Open) or 2 for NC (Normally close) depending on switching options.
2/ Output load capacity differential for NO and NC must be consider when using in same configuration.

TABLE VI. Input Parameters (SSR-C).

	Parameter
Max. Voltage ON	32 VDC
Nominal Voltage ON	28 VDC
Min. Voltage ON	18 VDC
Voltage Off (max)	+6 VDC
Typical Operating Current	25 mA
Typical Input Impedance	1.1 Kohms
Turn On Time Max	5 ms
Turn Off Time Max	3 ms

TABLE VII. Output Parameters and Load Capacity (SSR-C). 1/

	SSR1 (NO)	SSR2 (NC)
Max. Output Voltage	32 VDC or 28 VAC	
Min. Output Voltage	N/A	
Loads (AC/DC):		
On Resistance	Typical 0.2-ohm Max 0.5 ohm	Typical 1.0-ohm Max 2.5 ohm
Resistive	0.75 A	0.25 A
Inductive	0.5 A (300mH)	0.25 A (300mH)
Lamp	0.1 A(1A, 10ms. Inrush)	N/A
Audio	< 600 ohms	
Temperature Operating	-55 C to 85 C	
Temperature Non-Operating	-55 C to 85 C	

1/ Load tests performed at +85° C.

TABLE VIII. Signal Description.

Signals	Logic Functions Normally Open (SSR1)	Logic Functions Normally Closed (SSR2)
SW A, SW B, SW C, and SW D 2/	Shorted to COM A or COM B when the inputs (IN) are Active	Shorted to COM A or COMB when the inputs (IN) are not Active
Common	Signal COM A and COM B	
IN	Active when +28 VDC is applied across the inputs (IN) 1/	

Notes

1/ Input control circuits are bridge rectified and will respond to current flowing in either direction. Applications with reverse polarity sneak paths will require an external polarity protection diode.

2/ Outputs (A, B, C, and D) fused at 1.6 A and 0.5 A to protect against transients and overload conditions.

OEC Voltage Sensor (VS), Specifications:

Voltage Sensor is a solid- state, low-side direct current (DC) voltage sensor and may be configured for undervoltage or overvoltage detection. Voltage sensing is low drift over the specified temperature range. The Voltage Sensor compares positive DC voltage in a linear relationship between the specified setpoint and the voltage that is being monitored by the Sense Input (Pin 3). The OUT Z (Pin 1) provides a discrete signal that transitions from Open to Ground when the Sense Input (Pin 3) detects voltage that is above or below the specified setpoint. See Figure 7.

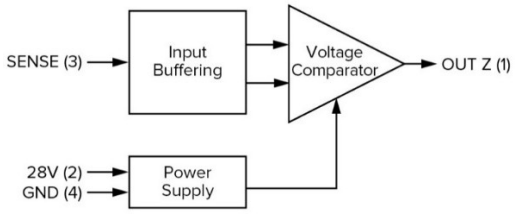


FIGURE 7. Voltage Sensor.

TABLE IX. Configuration (Voltage Sensor).

Type	Voltage Sense Values		Open Drain Output OUT Z (Pin 1)		Tolerances 1/ 2/
	Range	Increments	Active	Not Energized or inactive	
VSD2	50 to 90 mV	10mVDC	Ground	High Impedance (Open)	Nominal tolerance of a specified setpoint is +/- 5%. Voltage hysteresis band of +/- 1% around the setpoint, See Figures 10 and 11
	100 to 1000 mV DC	50mVDC			
VSD1	1 to 9 VDC	0.5 VDC			Nominal Rising Voltage Set Point Tolerance +/- 5%. Falling Voltage Hysteresis -3% Max (-2% Typical). See Figure 8 and 9.
	10 to 30 VDC	1 VDC			
	32 to 40VDC	2 VDC			
	44 to 48 VDC	4 VDC			

1/ Measured from the Set Point after the inclusion of the Rising Voltage Set Point Tolerance above.
2/ Tolerance of EMC and Environmental extremes is 10%.

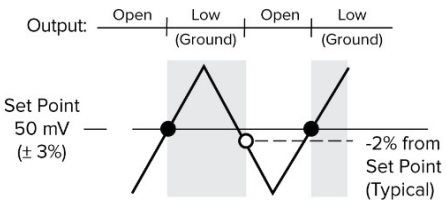


FIGURE 8. VSD1 - Overvoltage - Active Above SP.

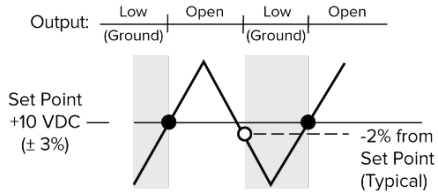


FIGURE 9. VSD1 - Undervoltage - Active Below SP.

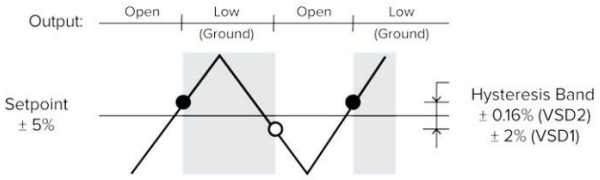


FIGURE 10. VSD2 - Overvoltage - Active Above SP.

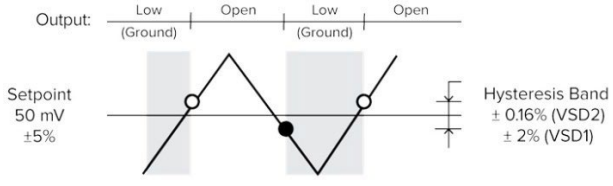


FIGURE 11. VSD2 - Undervoltage - Active Below SP.

TABLE X. Power and Input Parameters (Voltage Sensor).

Description	Parameters
Power Parameters	
Minimum Operating Voltage	+18 VDC
Maximum Operating Voltage	+32 VDC
Power Supply Current	2 mA Max.
Reset From Power Loss	5 second minimum @ +25° C
Hold Up On Power Loss	200 ms minimum
Input Parameters	
Minimum Sense Voltage	See range at Table IX
Maximum Sense Voltage	See range at Table IX
Rising Voltage Set Point Tolerance	See Tolerance at Table IX
Falling Voltage Hysteresis *Note: Measured from the Set Point after inclusion of the Rising Voltage Set Point Tolerance above.*	See Tolerance at Table IX
Transition Time Sense to Out (T_{Sense})	5 ms Max.
Input Impedance to unit ground	>1 Mohm

TABLE XI. Output Parameters and Load Capacity (Voltage Sensor). 1/

Output Parameters	VSD1 Output Parameters	VSD2 Output Parameters
Static Drain-Source On-State Resistance ($R_{DS(ON)}$)	48 mohm	600 mohm
Maximum Load (Resistive)	2.0 A	0.5 A
Maximum Load (Inductive)	0.8 A (300mH)	0.5 A (300mH)
Temperature		
Operating	-55° C to +85° C	
Non-operating	-55° C to +85° C	

1/ Load tests performed at +85° C.

Diode Pack (DP), Specifications:

Diode Pack (DP) are Series-A (4 Pin) components. Each Diode Pack component contains two independent diode circuits. See Figure 12.

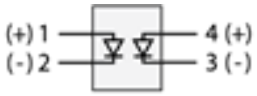


FIGURE 12. Diode Pack.

TABLE XII. Configuration (Diode Pack).

	DP2C	DP2M
Internal Didoes 1/	1N6484	1N5621JANTX
	glass passivized diodes	Hermetic glass sealed diodes

1/ Consult manufacturer's data sheet for detailed diode specifications.

TABLE XIII. Insulation Parameters (Diode Pack).

	DP2C DP2M
Insulation Resistance	5000 Megaohms @ 25° C
Dielectric Withstanding	1000 V_{RMS}

TABLE XIV. Electrical Parameters (Diode Pack).

	DP2C	DP2M
Current Rating (maximum)	1 Amp	1 Amp
Reverse Working Voltage	+1000 VDC	+800 VDC
Reverse Breakdown Voltage	+1000 VDC	+880 VDC Peak
Temperature Operating	-55 C to 85 C	
Temperature Non-Operating	-55 C to 85 C	

Terminal Block (TB), Specifications:

Terminal Block (TB) are Series-A (4 Pin) components. Each Terminal Block has a maximum of 5 Amps rating and provides the ability to buss a single input to three outputs. See Figure 13.

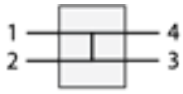


FIGURE 13. Single Configuration TB4.

TABLE XV. Insulation Parameters (Terminal Block).

	TB
Insulation Resistance	5000 Megaohms @ 25° C
Dielectric Withstanding	1000 V_{RMS}

TABLE XVI. Electrical Parameters (Terminal Block).

	TB
Current Rating (maximum)	5 Amp
Temperature Operating	-55 C to 85 C
Temperature Non-Operating	-55 C to 85 C

Electronic Latch (EL) , Specifications:

Solid State Electronic Latch (EL1, EL2), a Series-C (8 Pin) component, provides switching between orthogonal states.

EL1, EL2 input circuitry shall be diode isolated, buffered, and debounced. EL1, EL2 outputs shall be active ground open drain drivers both fused and surge-protected against transients and overload conditions.

EL1, EL2 provides two different operating modes by activating /SET, /RST, or /TGL. The switch then responds with conditioned outputs.

Latching circuitry holds the current state and provides /SET, /RST, and /TGL features along with a built-in blink (BLK) (1 Hz square wave) capability. See Figure 14.

TABLE XVII. Configuration (Electronic Latch).

		EL1	EL2
Power Up in		Reset	Set
At Power up	Q OUT	High (Open)	Low (Ground)
	/Q OUT	Low (Ground)	High (Open)
	BLINK	OFF (Open)	1 Hz (50% duty cycle) square wave alternating between High (Open) and Low (Ground)

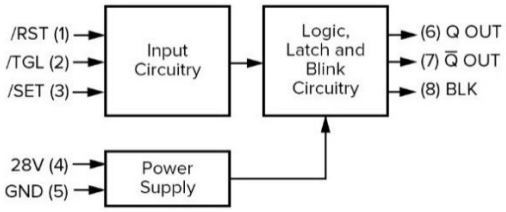


FIGURE 14. Electronic Latch.

TABLE XVIII. Signals Description (Electronic Latch).

Pin Ref	Signal Name	Function	Input Trigger or Active State	Description
1	/RST	Input	Low (Ground)	Forces Q OUTPUT to OFF (Open). Forces /Q OUT to ON (Ground). Forces BLK to Steady ON (Ground). 1/
2	/TGL	Input	↓ 3/	Toggles Q OUT and /Q OUT. Toggles blink mode. 2/
3	/SET	Input	Low (Ground)	Forces Q OUT to ON (Ground). Forces /Q OUTPUT to OFF (Open). Initiates the 1Hz blink mode to BLINK Output.
4	+28V	Power	–	Power (+18 VDC to +32 VDC)
5	GND	Common	–	Continuous Ground Required.
6	Q OUT	Output	Low (Ground)	Open Drain Output. Forced OFF (Open) by /RST Input. Forced ON (Ground) by /SET Input. Toggled by Falling Edge of /TGL Input.
7	/$\overline{Q}$ OUT	Output	Low (Ground)	Open Drain Output. Forced ON (Ground) by /RST Input. Forced OFF (Open) by /SET Input. Toggled by Falling Edge of /TOGGLE Input
8	BLK	Output	Low (Ground)	Open Drain Output. Forced ON (Ground) while /RST is held Low (Ground).

1/ BLK Output is held Steady ON (Ground) while /RST is held low. BLK Output goes OFF (Open) when /RESET returns to the inactive high level. This feature provides essentially three states to the BLINK Output: OFF, ON, and BLK. During EL1 Power-Up, /RESET is held low momentarily, which may result in a flicker of the indicator.

2/ TOGGLE input causes BLINK Output to switch between 1 Hz Blink state and OFF (Open). /TGL is overridden by /RST or /SET if they are active.

3/ Momentary toggle from High (Open) to Low (Ground) will flop Q OUT & /Q OUT to the opposite state.

TABLE XIX. Power Parameters (Electronic Latch).

	EL1 / EL2
Maximum Operating Voltage	+32 VDC
Nominal Operating Voltage	+28 VDC
Minimum Operating Voltage	+18 VDC
Power Supply Input Current	4 mA maximum
Reset From Power Loss	5 second minimum @ +25° C
Hold Up On Power Loss	50 ms minimum

TABLE XX. Input Parameters @ 25C (Electronic Latch). 1/

	EL1 / EL2
EL1: /RST, EL2: /SET	120 ms minimum
/TGL	45 ms minimum
EL1: /SET, EL2: /RST	45 ms minimum
High Level Input Voltage (V_{IH})	3 VDC minimum
Low Level Input Voltage (V_{IL})	0.4 VDC maximum
Low Level Input Current (I_{IL})	1 mA maximum

1/ All signal inputs are diode isolated

TABLE XXI. Output Parameters and Load Capacity (Electronic Latch). 1/

	EL1 / EL2
Loads:	
Resistive	2.0 A
Motor	1.0 A
Lamp	0.8 A
Inductive	0.8 A (300mH)
Temperature Operating	-55 C to 85 C
Temperature Non-Operating	-55 C to 85 C

1/Load tests performed at +85° C.

Electronic Rotary (ER1), Specifications:

Electronic Rotary (ER1), a Series-C (8 Pin) component, provides incremental switching through up to four latched output states. The number of latched states is user-defined and determined by routing the next highest output state back to the /RST input.

ER1 input circuitry shall be diode isolated, buffered, and debounced. ER1 outputs shall be Active ground open drain drivers both fused and surge-protected against transients and overload conditions.

The latching circuitry holds the current state until /INC or /RST inputs are toggled from High (Open) to Low (Ground). See Figure 15.

TABLE XXII. Configuration (Electronic Rotary).

		ER1
At Power up	/Q1	Low (Ground)
	/Q2	High (Open)
	/Q3	High (Open)
	/Q4	High (Open)

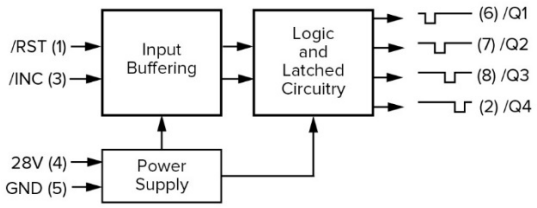


FIGURE 15. Electronic Rotary.

TABLE XXIII. Signals Description (Electronic Rotary).

Pin Ref	Signal Name	Function	Active State
1	/RST	Input Low-Resets to state 1 with /Q1 latched low when held low	
2	/Q4	Output: Default=High impedance (Open Drain) Becomes ground when state is active	
3	/INC	High to low transition advances the unit to the next state	Increment input at state 4 will return the unit to state 1
4	+28V	Power	
5	GROUND	Ground	Cont. Ground Req'd
6	/Q1	Output: High impedance (Open Drain) Becomes ground when state is active	
7	/Q2	Output: Default=High impedance (Open Drain) Becomes ground when state is active	
8	/Q3	Output: Default=High impedance (Open Drain) Becomes ground when state is active	

TABLE XXIV. Power Parameters (Electronic Rotary).

	ER1
Maximum Operating Voltage	+32 VDC
Nominal Operating Voltage	+28 VDC
Minimum Operating Voltage	+18 VDC
Power Supply Input Current	4 mA maximum
Reset From Power Loss	5 second minimum @ +25°C
Hold Up On Power Loss	50 ms minimum

TABLE XXV. Input Parameters at 25°C (Electronic Rotary). 1/

	ER1
/INC	50 ms minimum
/RST	80 ms minimum
Timing /INC to output	100 ms maximum
High Level Input Voltage (V_{IH})	3 VDC minimum
Low Level Input Voltage (V_{IL})	1.2 VDC maximum
Low Level Input Current (I_{IL})	1 mA maximum

1/ All signal inputs are diode isolated

TABLE XXVI. Output Parameters and Load Capacity (Electronic Rotary). 1/

	ER1
Loads:	
Resistive	2.0 A
Motor	1.0 A
Lamp	0.8 A
Inductive	0.8 A (300mH)
Temperature Operating	-55 C to 85 C
Temperature Non-Operating	-55 C to 85 C

1/ Load tests performed at +85° C.

Pulse Timer (PT1), Specifications:

Pulse Timer (PT1) is a Series-C (8 Pin) dual-channel edge detector and pulse generator. Each channel is independent and provides stable retriggerable/resettable one-shot operation for fixed timing applications. The trigger inputs allow rise and fall times that can be specified to sense either a rising-edge (Low to High) or falling-edge (High to Low) transition.

The PT1 can generate a wide range of timed pulse widths that are specified as either active High (Open) or active Low (Ground). Each channel includes a Low-triggered Reset Input for immediate termination of the pulsed Output.

PT1 input circuitry shall be diode isolated, buffered, and debounced. PT1 outputs shall be Active ground open drain both fused and surge-protected against transients and overload conditions.

The inputs must include an internal pull up to approximately +18 VDC. The PT1 requires constant power (+28 VDC) and Ground for proper operation. See Figure 16.

TABLE XXVII. Configuration (Pulse Timer) 1/.

	Trigger	Outputs	Pulse length options (+/- 10% at +25°C)
PT1	Positive (P)	Active High (H)	125 ms, 250 ms,
		Active Low (L)	500 ms, 1 sec
	Negative(N)	Active High (H)	2.5 sec 5 sec
		Active Low (L)	10 sec 20 sec

1/ Each of the two independent channels can be configure as per the table.

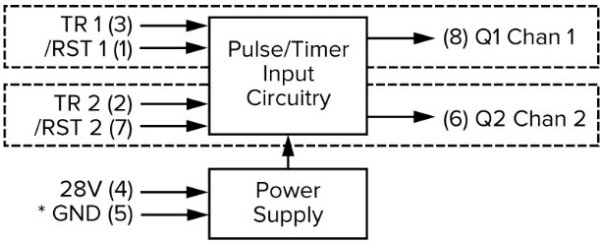


FIGURE 16. Pulse Timer.

TABLE XXVIII. Power Parameters (Pulse Timer).

	PT1
Operating Voltage (Max. / Nom. / Min.)	+32 VDC / +28 VDC / +18 VDC
Power Supply Input Current	4 mA maximum
Reset From Power Loss	5 second minimum @ +25°C
Hold Up On Power Loss	200 ms minimum

TABLE XXIX. Signals Description (Pulse Timer).

Input	Selected Input Option	Actual Input Received	Output Response	
			Q1 or Q2 Active High (Open) Normally Low ⎍	Q1 or Q2 Active Low (Ground) Normally High ⎍
TR 1 or TR2	Rising (Positive) Edge Detecting	Rising (Positive) ⌐	Output transitions from Ground to Open for the specified pulse period	Output transitions from Open to Ground for the specified pulse period
		Falling (Negative) ⌙	No Change: Output remains at Ground	No Change: Output remains at Open
	Falling (Negative) Edge Detecting	Rising (Positive)	No Change: Output remains at Ground	No Change: Output remains at Open
		Falling (Negative)	Output transitions from Ground to Open for the specified pulse period	Output transitions from Open to Ground for the specified pulse period
/RST 1 or /RSET 2	-	Reset = Open	Q1 and Q2 operate as defined above	
	-	Reset = Ground	Output is disabled (pulse cancelled) and is held at Ground	Output is disabled (pulse cancelled) and is held Open

TABLE XXX. Input Parameters at 25°C (Pulse Timer). 1/.

	PT1
/RESET (/RST)	55 ms minimum
TRIGGER (TR 1) (TR 2)	40 ms minimum
High Level Input Voltage (V_{IH})	5 VDC minimum
Low Level Input Voltage (V_{IL})	1.2 VDC maximum
Low Level Input Current (I_{IL})	1mA maximum

1/ All signal inputs are diode isolated

TABLE XXXI. Output Parameters and Load Capacity (Pulse Timer). 1/

	PT1
Loads:	
Resistive	2.0 A
Motor	1.0 A
Lamp	0.8 A
Inductive	0.8 A (300mH)
Temperature Operating	-55 C to 85 C
Temperature Non-Operating	-55 C to 85 C

1/ Load tests performed at +85° C.

Current Sensor (CS), Specifications:

Current Sensor (CS) is a solid-state, low-side direct current sensor. May be configure for undercurrent or overcurrent detection.

The CS compares electric current in a linear relationship between the specified setpoint and the current that is being monitored by the Sense Input. The output (OUT Z) provides a discrete signal that transitions from Open to Ground when the Sense Input detects current that is above or below the specified set point. See Figure 17.

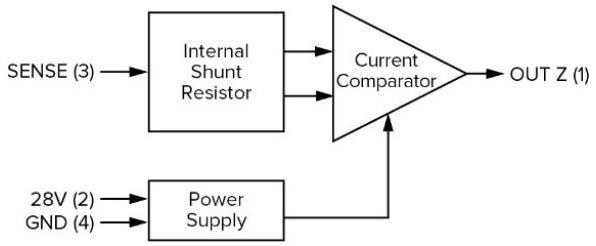


FIGURE 17. Current Sensor.

TABLE XXXII. Configuration (Current Sensor).

Type	Increments	Range	Open Drain Output (Pin 1)		Tolerances 1/
			Active	Not Energized or inactive	
CS1	10mA DC	10 to 90 mA DC	Ground	High Impedance (Open)	Nominal tolerance of a specified setpoint is +/- 5%. Hysteresis band of +/- 1% See Figures 18 and 19.
	50mA DC	50 to 1000 mA DC			

1/ Tolerance of specified Set Point is +/-10% at EMC and Environmental extremes.

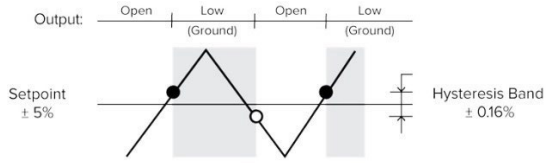


FIGURE 18. CS1 Overcurrent - Active Above SP

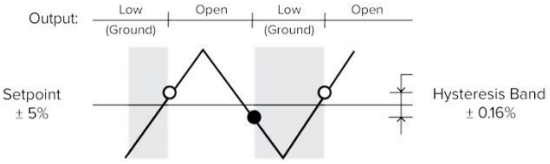


FIGURE 19. CS1 Undercurrent - Active Below SP

TABLE XXXIII. Power and Input Parameters (Current Sensor).

Description	Parameters
Power Parameters	
Operating Voltage (Max./Nom./ Min.)	+32 VDC /+28 VDC/+18 VDC
Power Supply Input Current	4 mA maximum
Reset From Power Loss	5 second minimum @ +25°C
Hold Up On Power Loss	50 ms minimum
Input Timing Input Impedance	10 ms maximum Approx. 100K Ohms
Input Parameters	
Minimum Sense Current	See Table XXXII
Maximum Sense Current	See Table XXXII
Transition Time Sense to Out (T_{Sense})	5 ms maximum

TABLE XXXIV. Output Parameters and Load Capacity (Current Sensor). 1/

Output Parameters	Output Parameters
Low Level Output	+0.4 VDC typical, +0.6 VDC maximum
High Level Output Voltage (VOH)	Open Drain +32 VDC maximum pull-up allowed
Maximum Load (Resistive)	0.5 A
Maximum Load (Inductive)	0.5 A (300mH)
Temperature	
Operating	-55° C to +85° C
Non-operating	-55° C to +125° C

1/ Load tests performed at +85° C.

Time Delay (TD) , Specifications:

Time Delay (TD1, TD2) is a Series-A (4-Pin) device with a range of timing options. The Input may be specified to detect a logic level (High/Low) as the event which triggers the Output to start the delay timer. Time Delay may also be specified to start the delay timer upon power-up. See Figure 20.

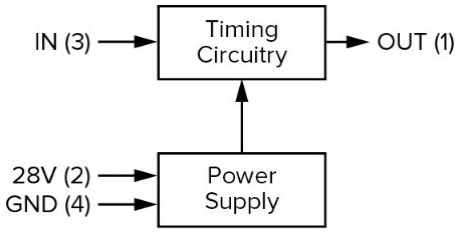


FIGURE 20. Time Delay.

TABLE XXXV. Configuration (Time Delay). 1/

Outputs	Time Delay starts	Stand-by	Delay Timing Options (+/- 5% at +25°C) 4/
TD1 (Ground when Active and Open when in Standby or Delay)	At Power UP 3/	Yes	• Milliseconds: 125*, 250*, 500 ms (*not available with the Time Delay on Power-up)
	On Trigger 2/	-	• Seconds: 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 15, 20, 30 sec
TD2 (Open when Active and Ground when in Standby or Delay)	At Power UP 3/	Yes	• Minutes: 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 15, 20, 30 min
	On Trigger 2/	-	• Hours: 1, 2, 4 hrs

1/ Each of the two independent channels can be configured as per the table.
2/ See Figures 20 and 21.
3/ See Figures 22 and 23.
4/ Tolerance of timing over temperature and EMC +/- 10%.

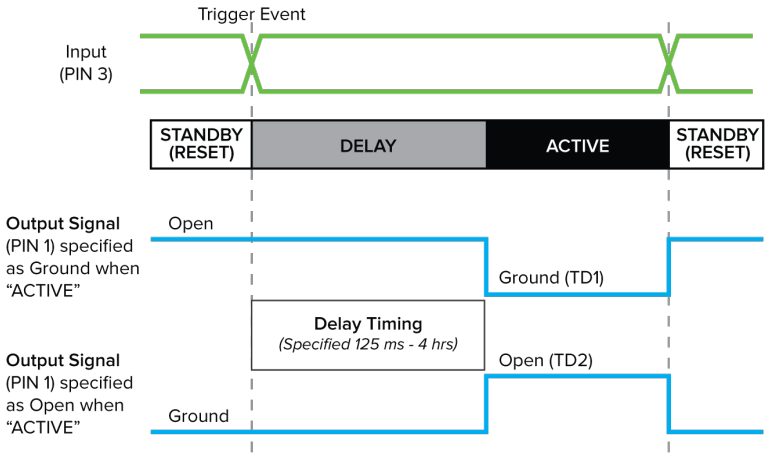


FIGURE 21. Time Delay on Trigger w/standby.

Transition Options for INPUT Level	
STANDBY	DELAY/ACTIVE
+28 VDC or Open	Ground
+28 VDC Must be same power source as PWR	Ground or Open
Ground or Open	+28 VDC Must be same power source as PWR
Ground	+28 VDC or Open

FIGURE 22. Transition Options.

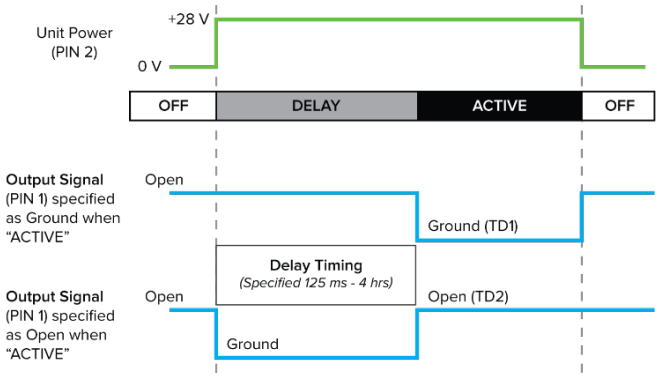


FIGURE 23. Time Delay on Power Up.

TABLE XXXVI. Power and input Parameters (Time Delay).

	TD
Operating Voltage (Max. / Nom. / Min.)	+32 VDC / +28 VDC / +18 VDC
Power Supply Input Current	4 mA maximum
Reset From Power Loss	5 second minimum @ +25°C
Hold Up On Power Loss	200 ms minimum

TABLE XXXVII. Input Parameters at 25° C (Time Delay). 1/

	TD
Input Timing	10 ms maximum
Low Level Input Current (IIL)	1 mA maximum
Low Level Input Voltage (VIL)	< +1.5 VDC
High Level Input Voltage (VIH)	> +8 VDC

1/ All signal inputs are diode isolated.

TABLE XXXVIII. Output Parameters and Load Capacity. 1/

	TD
Low Level Output Voltage @ 1A (VOL)	+0.4 VDC typical, +0.6 VDC maximum
High Level Output Voltage (VOH)	Open Drain +32 VDC maximum pull-up allowed
Loads:	
Resistive	0.5 A Max
Lamp/Incandescent	0.5 A
Inductive	0.5 A (300mH)
Temperature Operating	-55° C to 85° C
Temperature Non-Operating	-55° C to 125° C

1/ Load tests performed at +85° C.

Square Wave Oscillator (CT) , Specifications:

Square Wave Oscillator (CT1, CT2) is a Series-A (4-Pin) device with a range of oscillation frequency options. The Input may be specified to detect a logic level (High/Low) as the event which triggers the Output to begin oscillating. The Output continues oscillating until the trigger condition is reversed. See Figure 24 and Figure 25.

CT1, CT2 includes input circuity that is diode isolated, buffered, and debounced to provide reliable operation. The Output (Pin 1) is a High/Low (Open/Ground) driver that is fused and surge-protected against transients and overload conditions.

CT1, CT2 input circuitry shall be diode isolated, buffered, and debounced. CT1, CT2 outputs shall be High/Low driver fused and surge-protected against transients and overload conditions.

TABLE XXXIX. Configuration (Square Wave Oscillator). 1/

	Output		Delay Timing Options (+/- 5% at +25°C) 2/
	At Standby	When Active	Frequency / Period
CT1	Ground	Osc.	500 Hz / 0.002 sec 100 Hz / 0.01 sec 10 Hz / 0.10 sec 4 Hz / 0.25 sec
CT2	Open	Osc.	2 Hz / 0.50 sec 1 Hz / 1 sec 0.5 Hz / 2 sec 0.25 Hz / 4 sec

1/ Each of the two independent channels can be configure as per the table.
2/ Tolerance of timing over temperature and EMC +/- 10%.

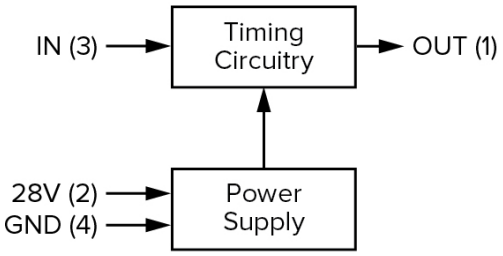


FIGURE 24. Square Wave Oscillator circuit.

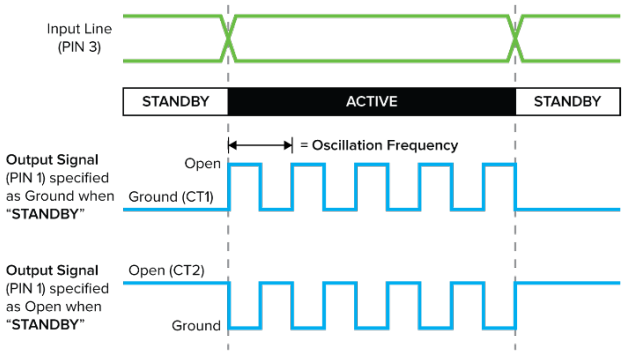


FIGURE 25. Square Wave Oscillator signal.

TABLE XL. Power Parameters (Square Wave Oscillator).

	CT
Operating Voltage (Max. / Nom. / Min.)	+32 VDC / +28 VDC / +18 VDC
Power Supply Input Current	4 mA maximum
Reset From Power Loss	5 second minimum @ +25°C
Hold Up On Power Loss	200 ms minimum

TABLE XLI. Input Parameters at 25°C (Square Wave Oscillator). 1/

	CT
Input Timing	10 ms maximum
Low Level Input Current (IIL)	1 mA maximum
Low Level Input Voltage (VIL)	< +1.5 VDC
High Level Input Voltage (VIH)	> +8 VDC

1/ All signal inputs are diode isolated.

TABLE XLII. Output Parameters and Load Capacity (Square Wave Oscillator). 1/

	CT
Low Level Output Voltage @ 1A (VOL)	+0.4 VDC typical, +0.6 VDC maximum
High Level Output Voltage (VOH)	Open Drain +32 VDC maximum pull-up allowed
Loads:	
Resistive	0.5 A Max
Lamp/Incandescent	0.5 A
Inductive	0.5 A (300mH)
Temperature Operating	-55° C to 85° C
Temperature Non-Operating	-55° C to 125° C

1/ Load tests performed at +85° C.

Defined Logic (DL), Specifications:

Defined Logic products are Series- C (8-Pin) component. It provides solid-state Boolean Logic control for use with digital circuit design. Each variation includes the ability to monitor up to four discrete inputs and drive two discrete outputs based on a logic decode of the inputs.

The Defined Logic interface handles Logic High and Logic Low levels that can be used to produce traditional Boolean Gates like AND, NAND, OR, NOR, EXOR, EXNOR, and NOT (Inverter).

The internal circuitry also performs the function of a signal Buffer. See Figure 26.

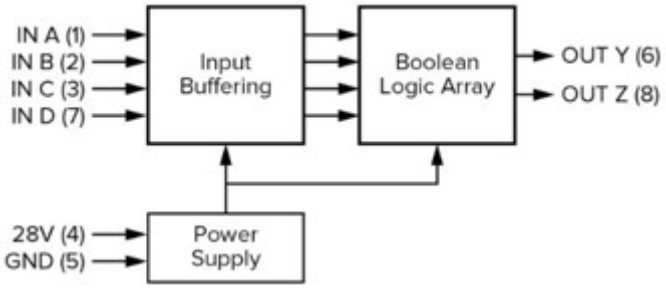
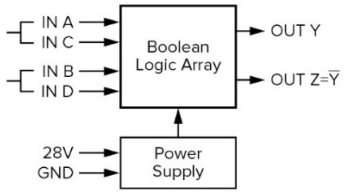
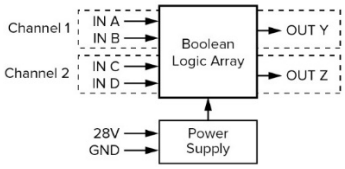
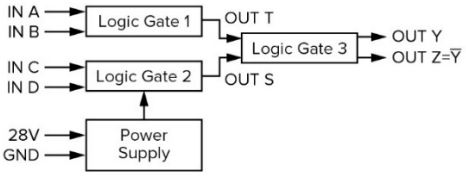
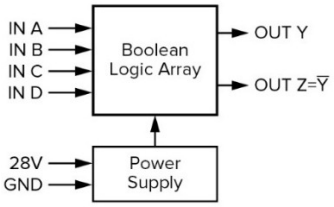


FIGURE 26. Defined Logic.

Configuration Options:
The Defined Logic (DL) Series consist of four configuration types and standard design characteristics that are common to each. Each Defined Logic configuration is comprised of four inputs (A - D) and two outputs (Y and Z). See Figure 26 and Table XLIII. The options vary among each type, and the following describes the unique characteristics which differentiate the four Defined Logic products.

TABLE XLIII. Configuration types (Defined Logic)

	Inputs A-D	Outputs	Available functions	Functional Diagram
DL1	two (tied) pairs	two orthogonal	TABLE XLIV	
DL2			TABLE XLV	
DL3			TABLE XLVI	
DL4	four discrete	provides two orthogonal outputs	TABLE XLVII	

Defined Logic (DL1): Monitor one set of inputs or the other when a signal is detected as active or not active, but not both. The DL1 output levels are specified as Logic High when both pairs of inputs are identical, and Logic Low when the pair of inputs differ.

The DL1 indicates when either one system or another is active or off, but not both. The DL1 will generate an Open (1) signal from output Y when both pairs of inputs are identical, and a Ground (0) signal when one pair is ground and the other pair is High Impedance. Output Z is orthogonal to Output. See Table XLIV.

For the DL1 variant only, input Pins A and C must be specified identically as either Pull-up or Pull-down since they must be externally tied together. Defined Logic (DL1) input options include specifying Pins A and C as Pull-up or Pull-down at the time of part configuration. See Input Level Options for Pins A and C.

TABLE XLIV. DL1 Functions.

Inputs		Outputs	
		("/XOR")	("XOR")
A, C	B , D	Y	Z
0	0	1	0
0	1	0	1
1	0	0	1
1	1	1	0
0 = Ground; 1 = Open (hi gh impedance)			

Defined Logic (DL2): The DL2 consists of dual (two) logically independent channels. Each channel consists of two inputs and a single output that is capable of providing one of ten types of Boolean Logic control. See Table XLIII and Table XLV.

Defined Logic (DL2) functions:

1) Boolean Logic decode (AND/OR/NAND/NOR, Logic Options 1-8), based on specific input level conditions to provide an output, specified as Ground (0) or Open (1),
2) Buffer output provides a filtered state of the input level,
3) Not (Inverter) output is orthogonal to the input level.

Defined Logic (DL2) input options include specifying Pins A and C as Pull-up or Pull-down at the time of part configuration. See Input Level Options for Pins A and C.

TABLE XLV. DL2 Functions.

Inputs		Y Output (Channel 1) Logic Options									
A	B	A • B	A • /B	/A • B	/A • /B	A + B	A + /B	/A + B	/A + /B	Buffer Y=A	Inverter Y=/A
0	0	0	0	0	**1**	**0**	1	1	1	0	1
0	1	0	0	**1**	0	1	**0**	1	1	0	1
1	0	0	**1**	0	0	1	1	**0**	1	1	0
1	1	**1**	0	0	0	1	1	1	**0**	1	0
Inputs		**Z Output (Channel 2) Logic Options**									
C	D	C • D	C • /D	/C • D	/C • /D	C + D	C + /D	/C + D	/C + /D	Buffer Z=C	Inverter Z=/C
0	0	0	0	0	**1**	**0**	1	1	1	0	1
0	1	0	0	**1**	0	1	**0**	1	1	0	1
1	0	0	**1**	0	0	1	1	**0**	1	1	0
1	1	**1**	0	0	0	1	1	1	**0**	1	0
0 = Ground; 1 = Open (high impedance)											

Defined Logic (DL3): The DL3 consists of a two-level cascaded Logic Gate that is controlled by combining the two outputs into a third Logic Gate that cascades the results of the two logically independent channels. See Table XLIII and Table XLVI.

Logic Gates 1 and 2 Functions:
1) Boolean Logic decode (AND/OR/NAND/NOR, Logic Options 1-8), based on specific input level conditions to provide an output, specified as Ground (0) or Open (1).
2) Buffer output provides a filtered state of the input level.
3) Not (Inverter) output is orthogonal to the input level.

Logic Gate 3 (Output Y) is normally Ground (0) until a single set of conditions exists on the outputs of Logic Gate 1 (Output T) and Gate 2 (Output S), as determined by the selected configuration from Table XLVI. Output Z is orthogonal to Output Y.

Defined Logic (DL3) input options include specifying Pins A and C as Pull-up or Pull-down at the time of part configuration. See Input Level Options for Pins A and C.

TABLE XLVI. DL3 Functions.

Inputs		Y, Z Output (Gate 3) Logic Options			
		T•S	T•/S	/T•S	/T•/S
T	S	Y,Z	Y,Z	Y,Z	Y,Z
0	0	0,1	0,1	0,1	**1,0**
0	1	0,1	0,1	**1,0**	0,1
1	0	0,1	**1,0**	0,1	0,1
1	1	**1,0**	0,1	0,1	0,1

0 = Ground; 1 = Open (high impedance)

Inputs		T Output (Gate 1) Logic Options									
A	B	A•B	A•/B	/A•B	/A•/B	A+B	A+/B	/A+B	/A+/B	Buffer T=A	Inverter T=/A
0	0	0	0	0	**1**	**0**	1	1	1	0	1
0	1	0	0	**1**	0	1	**0**	1	1	0	1
1	0	0	**1**	0	0	1	1	**0**	1	1	0
1	1	**1**	0	0	0	1	1	1	**0**	1	0
Inputs		**S Output (Gate 2) Logic Options**									
C	D	C•D	C•/D	/C•D	/C•/D	C+D	C+/D	/C+D	/C+/D	Buffer S=C	Inverter S=/C
0	0	0	0	0	**1**	**0**	1	1	1	0	1
0	1	0	0	**1**	0	1	**0**	1	1	0	1
1	0	0	**1**	0	0	1	1	**0**	1	1	0
1	1	**1**	0	0	0	1	1	1	**0**	1	0

0 = Ground; 1 = Open (high impedance)

Defined Logic (DL4): monitors and decode up to 4 discrete inputs and provides two orthogonal outputs. See Table XLIII. DL4 can also function as a 4-bit binary or binary-coded decimal (BCD) decoder.

The Output Y is normally Ground (0) until a single set of conditions exists on the four (A – D) discrete inputs.

When that single set of conditions occurs, Output Y will go Open (1). See Table XLVII. Output Z is orthogonal to Output Y. Output Z will remain Open (1) until the same set of conditions specified above occurs, at which time it will become Ground (0). See Table XLVII.

Defined Logic (DL4) input options include specifying Pins A and C as Pull-up or Pull-down at the time of part configuration. See Input Level Options for Pins A and C.

TABLE XLVII. DL4 Functions.

Inputs				Logic Options													
				A•B•C•D	A•B•C•/D	A•B•/C•D	A•B•/C•/D	A•/B•C•D	A•/B•C•/D	A•/B•/C•D	A•/B•/C•/D	/A•B•C•D	/A•B•C•/D	/A•B•/C•D	/A•B•/C•/D	/A•/B•C•D	/A•/B•C•/D	/A•/B•/C•D	/A•/B•/C•/D
				Outputs															
A	B	C	D	Y,Z	Y,Z	Y,Z	Y,Z	Y,Z	Y,Z	Y,Z	Y,Z	Y,Z	Y,Z	Y,Z	Y,Z	Y,Z	Y,Z	Y,Z	Y,Z
0	0	0	0	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	1,0
0	0	0	1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	1,0	0,1
0	0	1	0	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	1,0	0,1	0,1
0	0	1	1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	1,0	0,1	0,1	0,1
0	1	0	0	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	1,0	0,1	0,1	0,1	0,1
0	1	0	1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	1,0	0,1	0,1	0,1	0,1	0,1
0	1	1	0	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	1,0	0,1	0,1	0,1	0,1	0,1	0,1
0	1	1	1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	1,0	0,1	0,1	0,1	0,1	0,1	0,1	0,1
1	0	0	0	0,1	0,1	0,1	0,1	0,1	0,1	0,1	1,0	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1
1	0	0	1	0,1	0,1	0,1	0,1	0,1	0,1	1,0	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1
1	0	1	0	0,1	0,1	0,1	0,1	0,1	1,0	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1
1	0	1	1	0,1	0,1	0,1	0,1	1,0	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1
1	1	0	0	0,1	0,1	0,1	1,0	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1
1	1	0	1	0,1	0,1	1,0	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1
1	1	1	0	0,1	1,0	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1
1	1	1	1	1,0	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1
0 = Ground; 1 = Open (high impedance)																			

TABLE XLVIII. Power Parameters.

	DL1 to DL4
Operating Voltage (Max. / Nom. / Min.)	+32 VDC / +28 VDC / +18 VDC
Power Supply Input Current	4 mA maximum
Reset From Power Loss	5 second minimum @ +25°C
Hold Up On Power Loss	200 ms minimum

TABLE XLIX. Input Parameters at 25°C. 1/

	DL1 to DL4
Input Timing A, B, C & D	40 ms minimum
Low Level Input Current (IIL)	1 mA maximum
Low Level Input Voltage (VIL)	+1.2 VDC maximum
High Level Input Voltage (VIH)	+4 VDC minimum

1/ All Pulled-up signal inputs are diode isolated

TABLE L. Output Parameters and Load Capacity. 1/

	DL1 to DL4
Low Level Output Voltage @ 1A (VOL)	+0.4 VDC typical, +0.6 VDC maximum
High Level Output Voltage (VOH)	Open Drain +32 VDC maximum pull-up allowed
Loads:	
Resistive / Motor	2.0 A / 1.0 A Max
Lamp	0.8 A
Inductive	0.8 A (300mH)
Temperature Operating	-55° C to 85° C
Temperature Non-Operating	-55° C to 125° C

1/ Load tests performed at +85° C.

ARINC 429 Signal Converting

ARINC 429 Signal Converters consist of autonomous ARINC 429 IC Receivers and the protocol logic to decode and capture aa specified ARINC 429 data word, directly from the bus. The 32-bit data word is converted to an active digital signal(s), which becomes functional at the output(s), See Figure 27

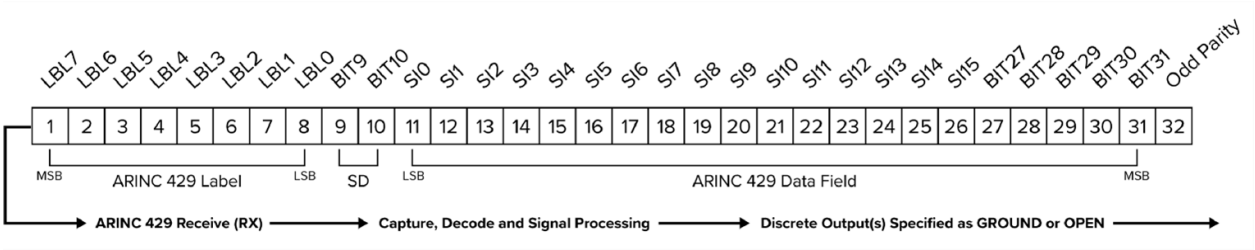


FIGURE 27. ARINC 429 Signal Processors Data to Discrete Sequence.

TABLE LII. Power Parameters (ARINC 429 Signal Converters).

	SR429 1M , 4M and 4D
Operating Voltage (Max. / Nom. / Min.)	+32 VDC / +28 VDC / +18 VDC
Power Supply Input Current	8 mA maximum
Reset From Power Loss	5 second minimum @ +25°C
Hold Up On Power Loss	200 ms minimum

TABLE LIII. Output Parameters and Load Capacity (ARINC 429 Signal Converters).

	SR429 1M	SR429 4M and 4D
Low Level Output Voltage @ 1A (VOL)	+0.4 VDC typical, +0.6 VDC maximum	+0.4 VDC typical, +0.6 VDC maximum
High Level Output Voltage (VOH)	Open Drain +32 VDC maximum	Open Drain +32 VDC Maximum
Loads:		
Resistive	1.0 A Max	0.5 A Max
Inductive	0.5 A (300mH)	0.5 A (300mH)
Temperature Operating	-55° C to 85° C	-55° C to 85° C
Temperature Non-Operating	-55° C to 125° C	-55° C to 125° C

Standard Output Characteristics

The three Signal Converter configuration types (SR429/1M, SR429/4M, and SR429/4D) provide up to three distinct output control activation options; Discrete Outputs, Decoded Outputs and the Failure Output (see below). All outputs are open-drain (High Impedance) when not active. The output load capacity is 1.0 A (Resistive) for the SR429/1M and 0.5 A (Resistive) for SR429/4M and SR429/4D.

Discrete Outputs: The Signal Converters each receive (RX) the ARINC 429 data transmission (TX), which is decoded and converted into active discrete output(s). One or more single (unary) bits can be converted into discrete outputs depending on the SR429 Signal Converter selected. There are two output options when converting a single ARINC data bit into a Discrete Output: Standard (High Impedance when data bit = 1) or Inverted (Ground when data bit =1). When data bit = 0 the output is orthogonal to the specified level when data bit = 1, see Table LIV.

TABLE LIV. Discrete Outputs.

Output Option	DATA BIT (Value)	DISCRETE OUTPUT (Signal Level)
Standard	1	High Impedance (High-Z)
	0	Ground (Low)
Inverted	1	Ground (Low)
	0	High Impedance (High-Z)

Decoded Outputs - Active outputs can also represent the decoding of multiple bits. Options for Decoded Outputs include a) the decoding of two data bits (producing 4 binary decode variations) or three data bits (producing eight binary decode variations) in the SR429/4D and b) the decoding of the Sign/Status Matrix bits (30, 31) producing four output variations available in the SR429/4M. The SSM decode allows data to represent functions typically defined as: 00 = Failure Warning (FW), 01 = No Computed Data (NCD), 10 = Functional Test (FT), and 11 = Normal Operation (NO).

Active Decoded Outputs can be specified as Ground or High Impedance when the decoded condition equals TRUE, see Table LV. Data bits that are specified for the BD function are positioned from MSB (Most Significant Bit) to LSB (Least Significant Bit). The MSB may also function as the sign bit in the two's complement operation to represent a negative value (i.e., - altitude,).

TABLE LV. Decoded Outputs.

Output Option	BINARY DECODE (Variation)	DECODED OUTPUT (Signal Level)
Ground when Decode Variation = TRUE	BD = TRUE	Ground (Low)
	BD = FALSE	High Impedance (High-Z)
High Impedance when Decode Variation = TRUE	BD = TRUE	High Impedance (High-Z)
	BD = FALSE	Ground (Low)

Failure Output - The Signal Converter is also designed to monitor the health of the internal IC receiver and offers two options for failure detection, Health and Watchdog, see Table LVI. Both options monitor the internal IC and produce an active output upon failure of the receiver IC and/or failure to receive valid ARINC data within a specified time buffer. The Health option also monitors loss of unit power.

Health and Watchdog include a buffer-timer that is intended to prevent signal chatter by inhibiting output activation until a specified time interval has elapsed. The timing is specified during part number configuration, and the options are 0.5s, 1.0s. 1.75s, 2.5s, 5.0s, 10.0s, 15.0s.

In the SR429/1M Signal Converter, only the Health version of the Failure Output is available which can be enhanced by combining additional external failure warnings into one active output.

TABLE LVI. Failure Output.

Output Option	IC (Status)	FAILURE OUTPUT (Signal Level)
Health	NORM	Ground (Low)
	FAIL	High Impedance (High-Z)
Watchdog	NORM	High Impedance (High-Z)
	FAIL	Ground (Low)

ARINC 429 Single Bit Converter (SR429/1M)

The ARINC 429 Single-Bit Converter (SR429/1M) is SERIES-N (8 Pins) component. The device consists of an autonomous ARINC 429 receiver and protocol logic that decodes and captures a specified ARINC 429 data word, directly from the bus. The 32-bit data word is converted into an active digital signal (Open or Ground), which becomes functional at the output.

The SR429/1M provides one active output (OUT), which is decoded from a single label and distinct bit, according to the ARINC 429 32-bit word protocol. A second output (FAIL) is available to allow for status indication of the internal Receiver IC, while simultaneously monitoring two additional inputs (IN 1, IN 2), which provide a failure interface for external discrete control of the Fail Sense Circuitry. See Figure 28.

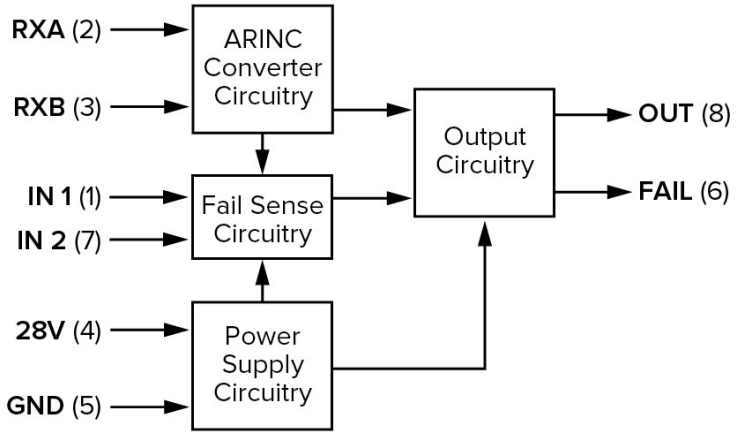


FIGURE 28. ARINC 429 Single-Bit Converter Circuitry.

TABLE LVII. ARINC 429 Single-Bit Converter.

Inputs	
28V	+18 VDC (Min), +28 VDC (Nom), +32 VDC (Max) Current Draw is 8mA maximum.
GRD	GND input must continually maintain a reference to Ground
RXA RXB	The two-wire data bus interface that autonomously receives the ARINC 429 unit of transmission (TX) directly from the data bus.
IN 1	IN 1 triggers the FAIL output (Pin 6) upon a fixed signal input level transition from Normal = High (High Impedance or > +20 VDC) to Fail = Low (ground or < +6 VDC). IN 1 may remain disconnected if unused.
IN 2	IN 2 triggers the FAIL output (Pin 6) upon one of two selectable signal input level transitions as described below. IN 2 must remain connected to the specified Normal signal level if unused. l From Normal = Low (ground or < +6 VDC) to Fail = High (high impedance or > +20 VDC) OR l From Normal = High (high impedance or > +20 VDC) to Fail = Low (ground or < +6 VDC). This option is similar to IN 1.
Outputs	
OUT	One Open-drain output, decoded from a single label and bit as defined by the ARINC 429, 32-bit data word protocol. The decoded Output ARINC 429 Bit can be: Output = Open when Bit =1 or Output = Ground when Bit = 1. When Bit = 0, outputs will be orthogonal to their specified state when Bit = 1.
FAIL	One Open-drain output, interfaced to the Fail Sense Circuitry monitoring the health of the internal Receiver IC and the status of two external discrete fail inputs (IN 1, IN 2). The level of the FAIL output is Fail = Open, Normal = Ground. The Fail Sense Circuitry may be bypassed if the failure output (FAIL) is unused.
Options	
Label	A single octal (base-8) label (000-377) specified from data bits 1 – 8, as defined by the ARINC 429, 32-bit data word format.
Data Bit	A single data bit (11 – 31) as defined by the ARINC 429, 32-bit data word format, can be selected for decoding by the Converter. Options include standard or inverted data bit.
SDI	Source/Destination Identifiers: Data bits 9 and 10 as defined by the ARINC 429, 32-bt word format. These bits are typically used for the identification of a data transmission source. At time of configuration, the SDI bits can be specified as Disabled (ignored) or Enabled (used as an extension of the Label) as valid for proper label identification as 00, 01, 10, or 11 for bits 9 and 10 respectively.
Tx Speed	Transmission Speed The speed by which the Converter receives the ARINC 429 unit of transmission, as defined by the ARINC 429-word protocol, is specified as either High speed (100 kbps) or Low speed (12.5 kbps).
Parity	Parity error detection includes a single check-bit (bit 32) to ensure correct data is received by checking for correct odd parity transmitted ARINC 429 words. The parity check option involves confirming that the total number of bits equal to 1 is calculated as an odd number, according to the odd parity system, as defined by the ARINC 429-word protocol. When the parity checking option is enabled, data will only be used if the parity is correct. When the parity checking option is disabled, the parity state is simply ignored.
Fail Sense Circuitry	
Health Monitor	The failure monitoring interface to the failure output (FAIL) allows for status indication when the following conditions occur: 1) failure of the Receiver IC, 2) loss of unit power 3) loss of ARINC data with the selected label for longer than the specified time buffer 4) Activation of the IN 1 or IN 2 failure inputs. The level of the Health Monitor output (FAIL) is: Fail = Open, Normal = Ground. The Health Monitor requires the specified ARINC 429 labels to be received within a specified time buffer. The buffer timing is specified during part number configuration, and the options are 0.5s, 1.0s. 1.75s, 2.5s, 5.0s, 10.0s, 15.0s

TABLE LVIII. Input Parameters at 25°C (ARINC 429 Single-Bit Converter).

	SR429 1M
IN 1, IN 2 Input Timing	5 ms (Typical)
IN 1, IN 2 Low Level Input Current (IIL)	1 mA maximum
IN1, IN2 Low Level Input Voltage (VIL)	< +6 VDC
High Level Input Voltage (VIH)	> +20 VDC

ARINC 429 Multi-Bit Converter (SR429/4M)

The ARINC 429 Multi-Bit Converter is a Series-N (8 Pins) or Series-R (12 Pins) signal converter. The device consists of an autonomous ARINC 429 receiver and protocol logic that decodes and captures a specified ARINC 429 data word, directly from the bus. The 32-bit data word is converted into an active digital signal(s) (Logic High = Open or Logic Low = Ground), which becomes functional at the output(s).

The SR429/4M provides four primary and four additional active outputs, see Figure 30 and 31. Each primary output represents a distinct bit, according to the ARINC 429 32-bit word protocol. The four additional outputs may include inverted data bit outputs, Health Monitor, Watchdog, or a binary decode of the SSM bits. See Table LIX.

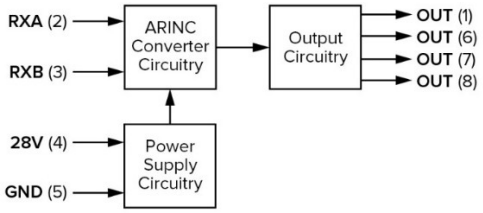


FIGURE 30. SR429/4M Series-N (8 Pins).

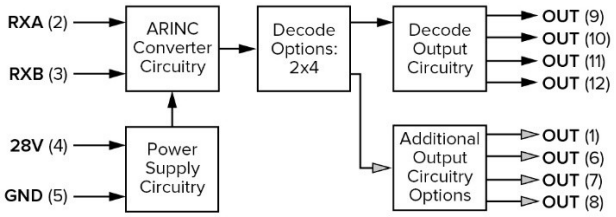


FIGURE 31. SR429/4M Series-R (12 Pins).

TABLE LIX. ARINC 429 Multi-Bit Converter.

Inputs	
PWR	+18 VDC (Min), +28 VDC (Nom), +32 VDC (Max) Current Draw is 8mA maximum.
GND	GND input must continually maintain a reference to Ground
RXA RXB	The two-wire data bus interface that autonomously receives the ARINC 429 unit of transmission (TX) directly from the data bus.
Outputs	
OUT Pins 1,6,7,8	Up to four outputs, as shown on FIGURE 30, selected from combinations of 1) specific decoded ARINC 429 data bits 11-31 2) Health Monitor (H), and 3) Watchdog (W). Each numeric ARINC 429 Bit can be specified at the time of configuration to be Output = Open when Bit = 1 or Output = Ground when Bit = 1. When Bit = 0, outputs will be orthogonal to their specified state when Bit = 1. Bits can be repeated or left unused. Health Monitor and Watchdog have defined output level.
OUT Pins 9,10,11,12	Four additional outputs, as shown on FIGURE 31, selected from combinations of 1) outputs related to the primary outputs, 2) Health Monitor (H), Health Monitor have defined output polarity 3) Watchdog (W). Watchdog have defined output polarity 4) SSM Decode outputs. SSM Decode outputs have level options when DECODE = TRUE. The use of additional outputs requires a Series R (12 Pin) ARINC 429 Multi-Bit Converter.
Standard Options	
Label	A single octal (base-8) label (000-377) specified from data bits 1 – 8, as defined by the ARINC 429, 32-bit data word format
Data Bit	Up to four unique bits from Bit 11 through Bit 31 as defined by the ARINC 429, 32-bit data word format, can be selected for decoding by the Converter. Options include standard or inverted data bit. See “Outputs” and TABLE LX.
SDI	Data bits 9 and 10 as defined by the ARINC 429, 32-bt word format. These bits are typically used for the identification of a data transmission source. At time of configuration, the SDI can be specified as Disabled (ignored) or Enabled (used as an extension of the Label) as valid for proper label identification as 00, 01, 10, or 11 for bits 9 and 10 respectively.
Tx Speed	The speed by which the Converter receives the ARINC 429 unit of transmission, as defined by the ARINC 429-word protocol, is specified as either High speed (100 kbps) or Low speed (12.5 kbps).
Parity	Parity error detection includes a single check-bit (bit 32) to ensure correct data is received by checking for correct odd parity on incoming ARINC 429 words. This involves confirming that the total number of bits equal to 1 is calculated as an odd number, according to the odd parity system, as defined by the ARINC 429-word protocol. When the parity checking option is enabled, data will only be used if the parity is correct. When the parity checking option is disabled, the parity state is simply ignored.
Additional Options	
Health Monitor	The failure monitoring interface to a specified failure output when the internal ARINC-429 receiver detects a 1) loss of power, 2) loss of valid data, or 3) an ARINC-429 receiver failure occurs. The Health Monitor failure output level is Open = Fail and requires the specified ARINC 429 label to be received within a specified time buffer. The buffer timing is specified during part number configuration, and the options are 0.5s, 1.0s. 1.75s, 2.5s, 5.0s, 10.0s, 15.0s.
Watchdog	The failure monitoring interface to a specified failure output when the internal ARINC-429 receiver detects a loss of valid data, or 2) an IC failure occurs. The Watchdog failure output level is Ground = Fail and requires the specified ARINC 429 label to be received within a specified time buffer. The buffer time is specified during part number configuration, and the options are 0.5s, 1.0s. 1.75s, 2.5s, 5.0s, 10.0s, 15.0s.

TABLE LX. SR429/4M Multi-Bit Converter Output Options.

	PRIMARY OUTPUTS				ADDITIONAL OUTPUTS			
Series	PIN 1	PIN 6	PIN 7	PIN 8	PIN 9	PIN 10	PIN 11	PIN 12
N	11-31, H or W	11-31, H or W	11-31, H or W	11-31, H or W	-	-	-	-
R	11-31, H or W	11-31, H or W	11-31, H or W	11-31	9	10 or H	11 or H	12 or H
	11-31, H or W	11-31, H or W	11-31, H or W	H or W	H or W	10 or H	11 or H	12 or H
	11-31, H or W	11-31, H or W	11-31, H or W	11-29	H or W	10 or H	11 or H	12 or H
R	11-29	11-29	11-29	11-31, H or W	SSM 00	SSM 01	SSM 10	SSM 11
	11-29	11-29	11-29	11-31, H or W	H or W	SSM 01	SSM 10	SSM 11
	11-29	11-29	11-29	11-31	9	SSM 01	SSM 10	SSM 11
	11-29	11-29	11-29	H or W	H or W	SSM 01	SSM 10	SSM 11

	OPTION DEFINITION
11-29, 11-31	For a single bit, 11-29 or 11-31 inclusive, Discrete Output can be specified as Standard (High Impedance when Bit = 1) or Inverted (Ground when Bit = 1)
H	Output is Open when Health Monitor = Fail
W	Output is Ground when Watchdog = Fail
9	For the same Bit specified in PIN 8, Output can be specified as Open when Bit = 1 or Ground when Bit = 1, regardless of the output level selection for PIN 8
10	For the same Bit specified in PIN 7, Output is Ground when Bit = 1, regardless of output level selection for PIN 7
11	For the same Bit specified in PIN 6, Output is Ground when Bit = 1, regardless of output level selection for PIN 6
12	For the same Bit specified in PIN 1, Output is Ground when Bit = 1, regardless of output level selection for PIN 1
SSM00 – SSM11	Binary Decode of SSM Bits (Bits 30 and 31), Binary Decode Output can be specified as Open when DECODE = TRUE or Ground when DECODE = TRUE

ARINC 429 Multi-Bit Decoder (SR429/4D)

The ARINC 429 Multi-Bit Decoder is a Series-N (8 Pins) or Series-R (12 Pins) signal converter. The device consists of an autonomous ARINC 429 receiver and protocol logic that decodes and captures a specified ARINC 429 data word, directly from the bus. The 32-bit data word is converted into an active digital signal(s) (Logic High = Open or Logic Low = Ground), which becomes functional at the output(s). The SR429/D decodes multiple ARINC 429 data-bits and includes two standard types of multi-bit decoding, 2X4 and 3X8.

ARINC 429 Multi-Bit Decoder's (SR429/4D) – Four or eight outputs, which are the binary decode of up to three data bits of a single label, according to the ARINC 429-word protocol. Additional options include Health Monitor and Watchdog. See Figures 31 and 32.

The SR429/4D has two standard types of decoding:

2 x 4 Decoder: unit provides a binary decode of two ARINC 429 data bits converted into four output signals, each corresponding to a single binary decode permutation (i.e. 00,01,10,11) The 2 X 4 Decoder can be configured as a Series-N (8 pin) or a Series-R (12 Pin) device as shown in Figure 32. The additional outputs options in a Series R device include 1) a specific decode of individual ARINC 429 bits (including the two individual bits used in the primary decode), 2) Health Monitor (H) and 3) Watchdog (W).

3 X 8 Decoder: unit provides a binary decode of two ARINC 429 data bits converted into eight output signals, each corresponding to a single binary decode permutation (i.e. 000,001, …, 111). The 3 X 8 Decoder can be configured as a Series-R (12 Pin) device as shown in Figure 33. The 3 x 8 Binary Decoder can be supplemented by replacing certain binary decoder outputs with options that include 1) a specific decode of individual ARINC 429 bits, 2) Health Monitor (H) and 3) Watchdog (W).

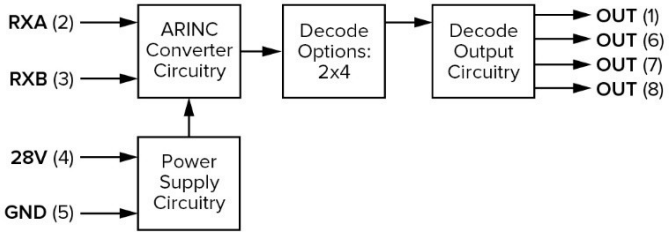


FIGURE 32. SR429/4D 2x4 Series-N or Series-R.

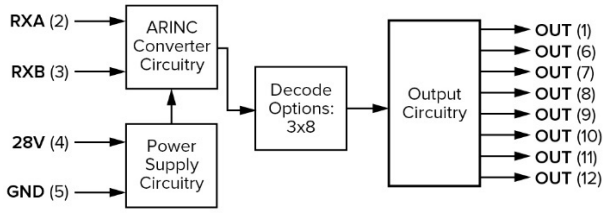


FIGURE 33. SR429/4D 3x8 Series-R.

TABLE LXI. ARINC 429 Multi-Bit Decoder.

Inputs	
28V	+18 VDC (Min), +28 VDC (Nom), +32 VDC (Max) Current Draw is 8mA maximum.
GRD	GND input must continually maintain a reference to Ground
RXA RXB	The two-wire data bus interface that autonomously receives the ARINC 429 unit of transmission (TX) directly from the data bus.
Outputs	
PRI 1 – 4 (2X4)	Outputs - 2 X 4 Decoder; Series N: A 2 X 4 Binary Decoder which provides four primary outputs, each is the binary decode (00, 01,10,11) of two bits according to the ARINC 429-word protocol. The 2 x 4 Binary Decoder can be supplemented by replacing the lowest permutation output (00) and/or the highest permutation output (11) with specific data, including 1) a specific decode of individual ARINC 429 bits, 2) Health Monitor (H) and 3) Watchdog (W).
ADD'L 1 – 4 (2X4)	Outputs – 2 x 4 Decoder; Series R: A 2 X 4 Binary Decoder which provides four primary outputs, each is the binary decode (00, 01,10,11) of two bits plus four additional output selections. The 2 x 4 Binary Decoder can be supplemented by replacing the lowest permutation output (00) with an additional output selection. These additional output options include 1) a specific decode of individual ARINC 429 bits (including the two individual bits used in the primary decode), 2) Health Monitor (H) and 3) Watchdog (W).
OUT 1 to 8 (3X8)	Outputs – 3 x 8 Decoder Series R: A 3 x 8 Binary Decoder which provides eight primary outputs, each is the binary decode (000 – 111) of three bits according to the ARINC 429-word protocol. The 3 x 8 Binary Decoder can be supplemented by replacing the lowest permutation output (000) and/or the highest permutation output (111) with specific data, including 1) a specific decode of individual ARINC 429 bits, 2) Health Monitor (H) and 3) Watchdog (W).
Standard Options	
Label	A single octal (base-8) label (000-377) specified from data bits 1 – 8, as defined by the ARINC 429, 32-bit data word format.
Data Bit	Up to four unique bits from Bit 11 through Bit 31 as defined by the ARINC 429, 32-bit data word format, can be selected for decoding by the Converter. Options include standard or inverted data bit. See "Outputs" and Tables LXII and LXIII.
SDI	Data bits 9 and 10 as defined by the ARINC 429, 32-bt word format. These bits are typically used for the identification of a data transmission source. At time of configuration, the SDI can be specified as Disabled (ignored) or Enabled (used as an extension of the Label) as valid for proper label identification as 00, 01, 10, or 11 for bits 9 and 10 respectively.
Tx Speed	The speed by which the Converter receives the ARINC 429 unit of transmission, as defined by the ARINC 429-word protocol, is specified as either High speed (100 kbps) or Low speed (12.5 kbps).
Parity	Parity error detection includes a single check-bit (bit 32) to ensure correct data is received by checking for correct odd parity on incoming ARINC 429 words. This involves confirming that the total number of bits equal to 1 is calculated as an odd number, according to the odd parity system, as defined by the ARINC 429-word protocol. When the parity checking option is enabled, data will only be used if the parity is correct. When the parity checking option is disabled, the parity state is simply ignored.
Additional Options	
Health Monitor	The failure monitoring interface to a specified failure output when the internal Receiver IC detects a 1) loss of power, 2) loss of valid data, or 3) an IC failure occurs. The Health Monitor failure output level is Open = Fail and requires the specified ARINC 429 labels to be received within a specified time buffer. The buffer timing is specified during part number configuration, and the options are 0.5s, 1.0s. 1.75s, 2.5s, 5.0s, 10.0s, 15.0s.
Watchdog	The failure monitoring interface to a specified failure output when the internal Receiver IC detects a loss of valid data, or 2) an IC failure occurs. The Watchdog failure output level is Ground = Fail and requires the specified ARINC 429 label to be received within a specified time buffer. The buffer time is specified during part number configuration, and the options are 0.5s, 1.0s. 1.75s, 2.5s, 5.0s, 10.0s, 15.0s

TABLE LXI. ARINC 429 Multi-Bit Decoder. - Continued

SSM	Sign/Status Matrix Decode: The binary decode of the two SSM data bits 30 – 31 (00, 01, 10, 11), converted into four output permutations. The output level of the decoded SSM outputs is specified during part number con- figuration as either Output = Ground when DECODE = TRUE or Output = Open when DECODE = TRUE. The SSM decode feature also offers bit selection options that will allow one additional converted output to replace (a.k.a., steal) the SSM decode answer 00. The steal option allows: 1) a repeat of the fourth primary bit, 2) the inverted form of the fourth primary bit (inverted output), 3) Health (H) or 4) Watchdog (W).
Binary Decoder Bit Selection	A 2 x 4 Binary Decoder converts two selected bits into four output permutations and a 3 x 8 Binary Decoder converts three selected bits into eight output permutations. Decoder bits are selected from ARINC 429 bits 11 – 31 or Watchdog (W) and can be arranged randomly or from Most Significant Bit (MSB) to Least Significant Bit (LSB) within the ARINC 429, 32-bit frame. The MSB may also represent a bit in the two's complement operation where 1 = negative, 0 = positive. The output level options of the binary decoder are: Output = Ground when DECODE = TRUE or Output = Open when DECODE = TRUE
Additional Bit Selections	Both the 2 x 4 Binary Decoder and the 3 X 8 Binary can be supplemented by replacing the lowest permutation output (00 or 000, respectively) and/or the highest permutation output (11 or 111, respectively) with specific ARINC 429 data bits. A 2 x 4 Decoder can have the bits used in the binary decode output as additional discrete bits. Each specific numeric ARINC 429 Bit can be specified at the time of configuration to be Output = Open when Bit = 1 or Output = Ground when Bit = 1. When Bit = 0, outputs will be orthogonal to their specified state when Bit = 1. Bits can be repeated or left unused. Health Monitor and Watchdog have defined output level. See "Outputs" for specifics on additional bit selections.

OUTPUTS

The output combinations consist of binary decoded data bits, specific data bits, Health Monitor (H) and Watchdog (W) as shown on Table LXII for 2 x 4 Decoders and Table LXIII for 3 x 8 Decoders.

The output level options of the binary decoder are: Output = Ground when DECODE = TRUE or Output = Open when DECODE = TRUE and is specified during part number configuration. All outputs are open-drain (Open).

TABLE LXII. SR429/4D Multi-Bit Converter (2x4) Output Options.

PRIMARY OUTPUTS				ADDITIONAL OUTPUTS			
PIN 1	PIN 6	PIN 7	PIN 8	PIN 9	PIN 10	PIN 11	PIN 12
D0	D1	D2	D3	-	-	-	-
11-29	D1	D2	D3	-	-	-	-
D0	D1	D2	11-31, H or W	-	-	-	-
11-29	D1	D2	11-31, H or W	-	-	-	-
11-29	MSB (11-31, H, W)	LSB (11-31, H, W)	11-31, H or W	D0	D1	D2	D3
11-29	MSB (11-31, H, W)	LSB (11-31, H, W)	11-31	9	D1	D2	D3
11-29	MSB (11-31, H, W)	LSB (11-31, H, W)	H or W	H or W	D1	D2	D3
11-29	MSB (11-31, H, W)	LSB (11-31, H, W)	11-29	H or W	D1	D2	D3

TABLE LXIII. SR429/4D Multi-Bit Converter (3X8) Output Options.

PRIMARY OUTPUTS							
PIN 1	PIN 6	PIN 7	PIN 8	PIN 9	PIN 10	PIN 11	PIN 12
D4	D5	D6	D7	D0	D1	D2	D3
D4	D5	D6	D7	11-31, H or W	D1	D2	D3
D4	D5	D6	11-31, H or W	D0	D1	D2	D3
D4	D5	D6	11-31	9	D1	D2	D3
D4	D5	D6	11-29, H or W	H or W	D1	D2	D3

OPTION DEFINITION	
11-29	For a single bit, 11 - 29 inclusive, Output can be specified as Open when Bit = 1 or Ground when Bit = 1
11-31	For a single bit, 11 - 31 inclusive, Output can be specified as Open when Bit = 1 or Ground when Bit = 1
H	Output is Open when Health Monitor = Fail
W	Output is Ground when Watchdog = Fail
9	Must be the same Bit specified in PIN 8
MSB	Most significant bit tied to initial MSB selection
LSB	Least significant bit tied to initial LSB selection
D0 – D7	BCD outputs for specified label & bits; output can be specified as Ground or Open when DECODE = TRUE

RS 232 / RS 422 Converter (RS422)

The RS 232 / RS 422 Converter (RS422) is SERIES-C (8 Pins) component. The device consists of an autonomous RS 232 and RS 422 receiver that converts RS 232 and RS 422 to RS 422 and RS 232, directly from and to the bus. The maximum data rate goes up to 115.2 kbps, for both RS 232 and RS 422. See Figure 29.

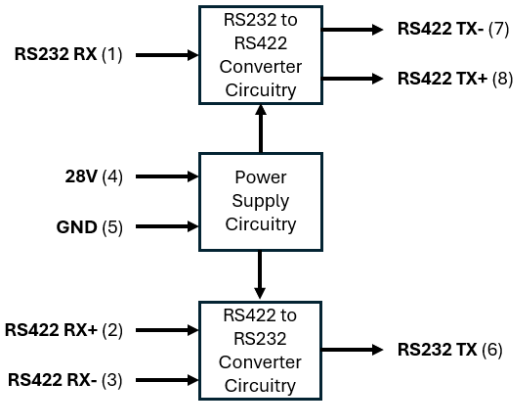


FIGURE 29. RS 232 / RS 422 Converter Circuitry

TABLE LXIV. RS 232 / RS 422 Converter.

Inputs	
28V	+18 VDC (Min), +28 VDC (Nom), +32 VDC (Max) Current Draw is 15 mA maximum.
GND	GND input must continually maintain a reference to Ground
RS232 RX	The RS232 received input. Directly connected to the data bus.
RS422 RX+	The RS422 received +. Directly connected to the data bus.
RS422 RX-	The RS422 received -. Directly connected to the data bus.
Outputs	
RS232 TX	The RS232 transmitted output. Directly connected to the data bus.
RS422 TX+	The RS422 transmitted +. Directly connected to the data bus.
RS422 TX-	The RS422 transmitted -. Directly connected to the data bus.

TABLE LXV. Power Parameters (RS 232 / RS 422 Converters).

	RS232/RS422
Operating Voltage (Max. / Nom. / Min.)	+32 VDC / +28 VDC / +18 VDC
Power Supply Input Current	15 mA maximum
Reset From Power Loss	8 VDC @ +25°C
Hold Up On Power Loss	200ms Minimum

TABLE LXVI. Output Parameters and Load Capacity (RS 232 / RS 422 Converters).

	RS232/RS422
High Level Output Voltage RS232 (RS232 TX)	> +2.5 VDC
Low Level Output Voltage RS232 (RS232 TX)	< -2.5 VDC
High Level Input Voltage RS422 (RS422 RX+ & RS422 RX-)	> 2.5 VDC
Low Level Input Voltage RS422 (RS422 RX+ & RS422 RX-)	< 50 mVDC
Bus Termination Loads:	
Resistive RS422	50mA (100 ohm)
Resistive RS232	500µA (10Kohm typ.)
Temperature Operating	-55° C to 85° C
Temperature Non-Operating	-55° C to 125° C

TABLE LXVII. Input/Output Signals Parameters at 25°C (RS 232 / RS 422 Converter).

	RS232/RS422
RS232 Input Rise/Fall Time (RS232 RX)	5 µs maximum
RS232 Low/High Level Input Current (RS232 RX)	125 µA maximum
RS232 Low/High Level Output Current (RS232 RX)	3.5 mA maximum
RS422 Input Timing (RS422 RX+ & RS422 RX-)	5 µs maximum
RS422 Low/High Level Input Current (RS422 RX+ & RS422 RX-)	125 µA maximum
RS422 Low/High Level Output Current (RS422 RX+ & RS422 RX-)	50 mA maximum
High Level Input Voltage RS232 (RS232 RX)	> +2.5 VDC
Low Level Input Voltage RS232 (RS232 RX)	< -2.5 VDC
High Level Input Voltage RS422 (RS422 RX+ & RS422 RX-)	> +2.5 VDC
Low Level Input Voltage RS422 (RS422 RX+ & RS422 RX-)	< 50 mVDC

TABLE LXVIII. Intentionally left blank

TABLE LXIX. Intentionally left blank

TABLE LXX. Intentionally left blank

Design and Construction: See Figures 1 through 5.

Functional Specifications: See TABLE I.

Materials:

Housing: High-temperature thermoplastic. EPOXY CARBON 3D EPX-82 .

Interconnect Pins: Base material to be copper alloy c36000 per ASTM B16/B16M (also known as cuzn36pb3), temper designation h02 (half hard). approved material sources are Swiss Metal and Wieland Metals. gold plate 50 to 120 microinches per SAE AMS 2422 over electrodeposited sulfamate nickel 50 to 150 microinches per SAE AMS -QQ-N-290.

Printed Circuit: Rigid, FR4; Flex, Kapton.

Weight:
Type A: 2 grams maximum
Type C: 3 grams maximum
Type N: 6 grams maximum
Type R: 6 grams maximum
Type S: 8 grams maximum

Shock II: High Impact Shock applicable only to OECs mounted in MIL-PRF-22885/108 pushbutton switches.

Insulation Resistance: Applicable between all leads of the OEC and a metal sleeve surrounding the OEC under test. High voltage shall not be applied between OEC leads.

Dielectric Withstanding: Applicable between all leads of the OEC and a metal sleeve surrounding the OEC under test. High voltage shall not be applied between OEC leads.

Environmental Performance See Table LXXXI

EMC/EMI Performance See Table LXXXII.

TABLE LXXI to LXXX. Intentionally left blank.

TABLE LXXXI. Environmental Performance for OECs.

Test Description	Test Parameters	Test Method	Units Compliant	Test parameter not applicable
Altitude (Low Pressure)	Functionally operate at the equivalent of 55,000 feet atmosphere for a minimum of 2 hours	RTCA/DO-160 Section 4, Category F2	All	
		MIL-STD-202-105, Test Condition B	All	
		MIL-STD 810 Method 500, Method III	All	
Overpressure	-15,000 feet, non-operational, 10 minutes	RTCA/DO-160 Section 4, Category A	All	
High Temperature Survivability and Operation, (operating)	+85ºC, 3 hours non-operating, followed by 2 hours operating	RTCA/DO-160 Section 4, level F2	All	
		MIL-STD-810 Method 501, Procedure II: 85°C	All	
Low Temperature Survivability and Operation	-55ºC, 3 hours non-operation, followed by 2 hours operational	RTCA/DO-160 Section 4, Level F2: -55°C	All	
		MIL-STD-810 Method 502, Procedure I: -55°C	All	
Thermal Shock	5 cycles at -55ºC and at +85ºC	RTCA/DO-160 Section 5, Category S2	All	
		MIL-STD-202-107,Category A	All	
		MIL-STD-810 Method 503, Method I-C	All	
High Temperature Survivability, (non-operating)	+125ºC, 96 hours	MIL-STD-202-108, Category A	All	
Humidity, (Non-operating)	240 hours, +65ºC, >90% RH	RTCA/DO-160 Section 6	All	
		MIL-STD-202-106	All	
Humidity (Operating)	240 hours, +65°C, 95% RH	MIL-STD-810 Method 507, Procedure II	All	
Acceleration	20G acceleration, 3 axes each orientation, 3 seconds each	RTCA/DO-160 Section 7, Category B	All	
	20G constant acceleration, 3 axes each orientation, 5 minutes each, total of 30 minutes	MIL-STD-202-212 Test Condition A	All	
	≤ 20G acceleration, 1 minute per aircraft load condition (6 total)	MIL-STD-810 Method 513 Procedure III	All	
Operational Shock and Crash Safety	20G Saw-tooth, 11ms	RTCA/DO-160 Section 7 Category B	All	
	75G Half-sine	MIL-STD-810 Method 516	All	
	75G Half-sine	MIL-STD-202-213	All	
Vibration	10-2000Hz, 10G	RTCA/DO-160G Section 8	All	
	10-2000Hz, 15G peak	MIL-STD-202-204, Condition B	All	

TABLE LXXXI Environmental Performance for OECs . continued

Test Description	Test Parameters	Test Method	Units Compliant	Test parameter not applicable
Explosive Atmosphere	Non-ignition test at site level pressure	RTCA/DO-160 Section 9, Category E	All	
	multiple altitudes from 5,000 to 60,000 feet with gasoline explosion	MIL-STD-202-109, Level B	All	
Waterproofness Seal (Sealed Switch Only)	Condensing Waterproof Test	RTCA/DO-160 Section 10, Level Y	All	When standalone unsealed
Waterproofness Seal (Sealed Switch Only), continued	Drip Proof Test	RTCA/DO-160 Section 10, Level W	All	When standalone unsealed
Sand and Dust	Silica media	RTCA/DO-160 section 12, Level D	All	
		MIL-STD-202-110	All	
Fungus Resistance	Compliance by material selection	RTCA/DO-160 Section 13, Level F	All	
		MIL-PRF-22885 3.5.2	All	
Salt Fog	96 hour test	RTCA/DO-160 Section 14, Level T	All	
		MIL-STD-202-101, Level A	All	

TABLE LXXXII. EMC/EMI Requirements for OECs.

Test Description	Test Parameters	Test Method	Units Compliant	Test parameter not applicable
Magnetic Effect	1° deflection, 0-0.3m	RTCA/DO-160 Section 15, Level Z	All	Magnetic Effect
Power Input	Aircraft Power: 18 to 32.2VDC,	RTCA/DO-160 Section 16.6.1.1, Category A: Aircraft Power	All	DP, TB
	Power Interrupt: up to 50ms	RTCA/DO-160 Section 16.6.1.3, Category B: Power Interrupt	All	DP, TB
	Power Interrupt: up to 200ms	RTCA/DO-160 Section 16.6.1.3, Category A: Power Interrupt	All except as indicated	EL1, EL2, SR429/1M, DP, TB
	Normal Surge Voltage: 47VDC, 5ms; 40VDC, 30ms	RTCA/DO-160 Section 16.6.1.4, Category A: Normal Surge Voltage	All	DP, TB
	Engine Start Under Voltage: ramp input voltage from 10VDC to 28VDC in 35 seconds	RTCA/DO-160 Section 16.6.1.5, Category B: Engine Start Under Voltage	All	DP, TB
	Low Voltage Condition: decrease power from nominal to 0VDC over a 10-minute period	RTCA/DO-160 Section 16.6.2.2, Category B: Low Voltage Condition	All	DP, TB
	Momentary Under Voltage: 12VDC operation for 7 seconds	RTCA/DO-160 Section 16.6.2.3, Category A: Momentary Under Voltage	All	DP, TB
	Abnormal Surge Voltage: 46.3VDC for 100ms, 37.8VDC for 1 second.	RTCA/DO-160 Section 16.6.2.4, Category A: Abnormal Surge Voltage	All	DP, TB
	Abnormal Surge Voltage: 60VDC for 100ms, 40VDC for 1 second.	RTCA/DO-160 Section 16.6.2.4, Category B: Abnormal Surge Voltage	All	DP, TB
	Voltage and Surge: 22-29V, 0.035V maximum, 1.5V maximum ripple	MIL-STD-704: 22-29V, 0.035V maximum, 1.5V maximum ripple	All	DP, TB
Voltage Spike	600V, 10µs, 50Ω	RTCA/DO-160 Section 17,Level A	All	
	400V, 10µs, 5Ω	MIL-STD-461 CS106, Spike 1	All	
Audio Frequency Conducted Susceptibility	Power Input, 4V P-P ripple, 0.01 -150 KHz	RTCA/DO-160 Section 18, Level Z:	All	DP, TB
	30Hz to 150kHz, 126dB µV	MIL-STD-461 CS101, Curve 2	All	DP, TB
Induced Signal Susceptibility	10,000V/m, 120A/m, 350-800Hz	RTCA/DO-160 Section 19, Level CW	All	DP, TB
RF Susceptibility (Conducted)	500mA, 10kHz-400MHz	RTCA/DO-160 Section 20, Level Y	All	DP, TB
RF Susceptibility (Conducted),	109 dBuA, 10kHz-200MHz	MIL-STD-461 CS114, Curve 5	All	DP, TB
RF Susceptibility (Radiated), continued	200V/m, 2MHz-18GHz	RTCA/DO-160 Section 20 Level Y	All	DP, TB
	200 V/m , 2MHz-18GHz	MIL-STD-461 RS103: 200 V/m	All	DP, TB
RF Emissions (Conducted)	150kHz-152MHz	RTCA/DO-160 Section 21, Level P	All	DP, TB
	10kHz-10MHz	MIL-STD-461 CE102	All	DP, TB

TABLE LXXXII. EMC/EMI Requirements for OECs. continued

Test Description	Test Parameters	Test Method	Units Compliant	Test parameter not applicable
RF Emissions (Radiated)	150kHz- 6MHz	RTCA/DO-160 Section 21, Level P: 150kHz-6MHz	All	DP, TB
	10 kHz- 6GHz	MIL-STD-461 RE102	All	DP, TB
Military Transients	30 ns, 5A	MIL-STD-461 CS115	All	DP, TB
	500V, Damped Sinusoidal, 10 KHz to 120 MHz	MIL-STD-461 CS116	All	DP, TB
Lightning Induced Transient	Waveform 3, 600V, 1MHz, 10Mhz	RTCA/DO-160 Section 22, Category XXK3L3	All	DP, TB
	Waveform 4, 300V, 69µs	RTCA/DO-160 Section 22, Category XXK3L3	All	DP, TB
	Waveform 5A, 300V, 120µs	RTCA/DO-160 Section 22, Category XXK3L3:	All	DP, TB
	Waveforms 3, 4 and 5A	MIL-STD-461 CS117	All	DP, TB
Dielectric Withstanding	1000VAC	MIL-STD-202-301	All	
Electrostatic Discharge	15,000V, 150pf, 330Ω	RTCA/DO-160 Section 25	All	DP, TB
		MIL-STD-461 CS118	All	DP,TB

Table LXXXIII. Qualification Table.

Test Sample	Group	Number of samples	Additional Testing	Req of Additional Testing
M22885/117ATD1	I II III	2 2 2	2 EMI/EMC 2 Altitude/ Over Pressure 2 High Temp Survival (operating) 2 Low Temp Survival 2 High Temperature survivability (non-operating)	*MIL-PRF-22885/117 Table LXV *MIL-STD-810: 500.6-II; DO-160: 4.6.1, 4.6.3-F2, A2 *DO-160: 4.5.3,4.5.4-F2 *DO-160: 4.5.1-F2 *MIL-STD-202-108
M22885/117ASR1	I II III	2 2 2	3 EMI/EMC 2 Altitude/ Over Pressure 2 High Temp Survival (operating) 2 Low Temp Survival 2 High Temperature survivability (non-operating)	* MIL-PRF-22885/117 Table LXV *MIL-STD-810: 500.6-II; DO-160: 4.6.1, 4.6.3-F2,A2 *DO-160: 4.5.3,4.5.4-F2 *DO-160: 4.5.1-F2 *MIL-STD-202-108
M22885/117CEL1	I II III	8 2 2	4 EMI/EMC 2 Altitude/ Over Pressure 2 High Temp Survival (operating) 2 Low Temp Survival 2 High Temperature survivability (non-operating)	* MIL-PRF-22885/117 Table LXV *MIL-STD-810: 500.6-II; DO-160: 4.6.1, 4.6.3-F2, A2 *DO-160: 4.5.3,4.5.4-F2 *DO-160: 4.5.1-F2 *MIL-STD-202-108
M22885/117CCR	I II III	8 2 2	5 EMI/EMC 2 Altitude/ Over Pressure 2 High Temp Survival (operating) 2 Low Temp Survival 2 High Temperature survivability (non-operating)	* MIL-PRF-22885/117 Table LXV *MIL-STD-810: 500.6-II; DO-160: 4.6.1, 4.6.3-F2,A2 *DO-160: 4.5.3,4.5.4-F2 *DO-160: 4.5.1-F2 *MIL-STD-202-108
M22885/117NSC	I II III	2 2 2	6 EMI/EMC 2 Altitude/ Over Pressure 2 High Temp Survival (operating) 2 Low Temp Survival 2 High Temperature survivability (non-operating)	* MIL-PRF-22885/117 Table LXV *MIL-STD-810: 500.6-II; DO-160: 4.6.1, 4.6.3-F2, A2 *DO-160: 4.5.3,4.5.4-F2 *DO-160: 4.5.1-F2 *MIL-STD-202-108
M22885/117RMD	I II III	2 2 2	7 EMI/EMC 2 Altitude/ Over Pressure 2 High Temp Survival (operating) 2 Low Temp Survival 2 High Temperature survivability (non-operating)	* MIL-PRF-22885/117 Table LXV *MIL-STD-810: 500.6-II; DO-160: 4.6.1, 4.6.3-F2, A2 *DO-160: 4.5.3,4.5.4-F2 *DO-160: 4.5.1-F2 *MIL-STD-202-108

Group I: Visual and Mechanical examination, Solderability, Operating characteristics.
Group II: Thermal Shock, Shock, Vibration, Moisture Resistance, operating characteristics and Marking Visibility.
Group III: Salt-Spray, Insulation Resistance and Operating characteristics.

TABLE LXVIII. Group B Inspection testing.

		Series A		Series C								Series C								Series N		Series R	
Test description	**Per Spec**	**S1**	**S2**	**S3**	**S4**	**S5**	**S6**	**S7**	**S8**	**S9**	**S1**	**S11**	**S1**	**S13**	**S1**	**S1**	**S16**	**S1**	**S1**	**S19**	**S2**	**S2**	**S22**
Visual and mechanical	**MIL-PRF-22885: 4.7.1**	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Solderability	**MIL-PRF-22885 4.7.2**		X					X	X							X	X			X	X		X
EMI/EMC	**Mil-PRF-22885/117 Table LXV**	X	X	X	X																	X	X
Altitude/ Over Pressure	**MIL-STD-810: 500 Met III; DO-160 Sec 4, Cat F2:**	X	X	X	X							X	X							X	X	X	X
High Temp Survival (operating)	**DO-160: 4.5.3,4.5.4-F2**	X	X	X	X							X	X							X	X	X	X
Low Temp Survival	**MIL-STD-810:502 Proc I; DO-160: Sec 4.5.1 cat F2**	X	X	X	X							X	X							X	X	X	X
High Temperature survivability (non-operating)	**MIL-STD-202-108 Cat. A**	X	X	X	X							X	X							X	X	X	X
Thermal Shock	**MIL-PRF-22885: 4.7.14**	X	X			X	X							X	X					X	X	X	X
Shock I	**MIL-PRF-22885: 4.7.16.1; MIL-STD 202: 213B; MIL-STD-810: 516.6-V; DO-160: 7.1.1B; DO-160: 7B-2-5; MIL-STD-202: 212A; MIL-STD-810:513-II**	X	X			X	X							X	X					X	X	X	X
Vibration	**DO-160: 8R-C,C1,U,G; MIL-PRF-22885: 4.7.15; MIL-STD-202: 204B**	X	X			X	X							X	X					X	X	X	X
Insulation Resistance	**MIL-PRF-22885: 4.7.23**	X	X			X	X							X	X					X	X	X	X
Moisture resistance	**MIL-STD-810: 507.5-II**	X	X			X	X							X	X					X	X	X	X
Insulation Resistance	**MIL-PRF-22885: 4.7.23**	X	X			X	X			X	X			X	X			X	X	X	X	X	X
Salt spray	**MIL-PRF-22885: 4.7.22; DO-160: Sec 14 Level T**	X	X					X	X							X	X			X	X	X	X
Operating characteristics	**MIL-PRF-22885: 4.7.6**	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Marking Visibility	**MIL-PRF-22885: 4.7.21**	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

TABLE LXIX. Series Samples.

Samples Series	MFG ID (see table 1)	MIL-ID
Series A (samples 1 and 2)	TD1	M22885/117ATD1
	SR1H	M22885/117ASR1
Series C (Samples 3 to 10)	EL1	M22885/117CEL1
Series C (Samples 11 to 18)	SSCR	M22885/117CCR
Series N (Samples 19 to 20)	SR429/1M	M22885/117NSC
Series R (Samples 21 to 22)	SR429/4D	M22885/117RMD

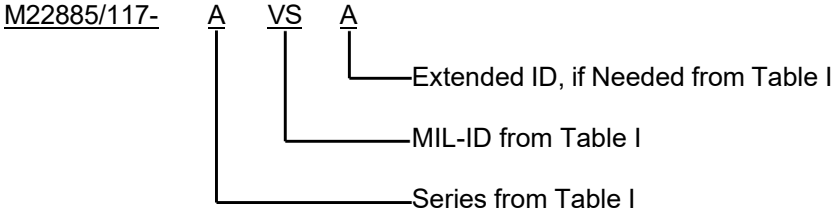
Table LXX. Group A inspection.

Visual and mechanical examination (Size and weight) 1/
Operating characteristics2/
Dielectric withstanding voltage. 3/

1/ To be performed on each Lot and by Series of products.
2/ Functional Test at typical operating voltage.
3/ Applicable between all leads of the OEC and a metal sleeve surrounding the OEC under test. High voltage shall not be applied between OEC leads.

Part or Identifying Numbers (PIN): PIN's are assigned as follows:

Example: Solderable OEC, Voltage Sensor, Activation Above, 10V:



The part marking of solderable OECs procured to this specification shall include the specification number and OEC Series and Mil-ID per table 1. Supplementary information pertinent to the specified OEC shall be included only when available in column Extended ID of Table I.

OECs procured with MIL-PRF-22885/108 and MIL-PRF-22885/113 pushbutton switches shall follow placement and part marking requirements specified therein and may be different than what is described herein.

The margins of this specification are marked with vertical lines to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the previous issue.

Referenced documents:

- MIL-PRF-22885
- MIL-PRF-22885/108
- MIL-PRF-22885/113
- MIL-PRF-22885/116
- MIL-STD-202-101
- MIL-STD-202-105
- MIL-STD-202-106
- MIL-STD-202-107
- MIL-STD-202-108
- MIL-STD-202-109
- MIL-STD-202-110
- MIL-STD-202-204
- MIL-STD-202-212
- MIL-STD-202-213
- MIL-STD-202-301
- MIL-STD-461
- MIL-STD-704
- MIL-STD-810
- ASTM B16/B16M
- RTCA/DO-160
- SAE AMS 2422
- SAE AMS-QQ-N-290

Custodians:
Army – CR
Navy - EC
Air Force - 85
DLA - CC

Preparing Activity:
DLA - CC

(Project 5930-2024-061)

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.dla.mil/ .